**FFT/IFFT Processor** IP Core
Customizable FFT/IFFT core for the OFDM systems

### General description

**FFT/IFFT Processor** is an IP Core for the implementation of both the FFT and the IFFT components in an OFDM system.

**FFT/IFFT Processor** main features:
- The choice of forward or inverse transform is run-time configurable. Thus, it can be implemented on OFDM transmitters, receivers and transceivers.
- It is a flexible solution that can be customized for any OFDM application.
- It is based on a pipeline architecture.
- It can implement both fixed-length and variable-length FFT/IFFTs.
- It offers an excellent trade-off between latency time and FPGA resources.
- It is a full hardware solution that can be implemented on low-cost Xilinx FPGAs.

### Applications

**FFT/IFFT Processor** may be used in a wide range of OFDM applications. It allows a seamless integration in low-cost and high end FPGA families. Among other technologies and standards where **FFT/IFFT Processor** can be directly used, we can highlight:

- Ultra-Wide Band (UWB)
- Digital Video Broadcasting (DVB)
- Wireless Local Area Network (WLAN)
- Worldwide Interoperability for Microwave Access (WiMAX)
- Long Term Evolution (LTE)

Additionally, **FFT/IFFT Processor** can be used in other kinds of applications, such as correlations, spectral analysis, frequency analysis or vibration analysis.

### Standard package features

**FFT/IFFT Processor** standard package includes the following items:

- IP core netlist ready for seamless integration in ISE design flow
- Reference design for Xilinx Spartan-6 LXT family FPGA
- Full testbenches with stimuli data
- Customization of the IP core depending on the needed specifications: number of FFT/IFFT points, quantization, latency time, available FPGA resources...
Application examples

This example presents a configuration of the FFT/IFFT Processor FFT/IFFT IP core for the DVB-T standard. It has been selected a radix $2^7$ pipeline-SDF DIF architecture for the 8K-points mode of DVB-T.

The input and output data are vectors of $N$ complex values, being $N$ the number of points of the FFT/IFFT processor. As it is a DIF algorithm, input data is presented in natural order and the output data in bit reversed order.

The BF1 blocks implements the hardware needed to perform the arithmetic operations of the radix 2 butterflies and the required shuffling for its correct operation. The BF2 blocks are similar to the BF1 blocks. However, some of the outputs are multiplied by $-j$.

When the number of different twiddle factors corresponding to a twiddle factor operator is small, its implementation is improved with constant multipliers. In other cases, a complex multiplier and a ROM are used.

About the company

SoCe offers specialized design services of FPGAs, SoPCs, IPs and embedded systems. It focuses on FPGA based Ruggedized Systems, Industrial Networking and Video processing.

Ordering information and contact

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