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CPPS - Gate40

Redbox

High-availability and synchronization for SAS

General Description

The new era in Smart Grid demands interconnecting heterogeneous systems, high computational capacity and flexible interfaces with the "physical" world.

CPPS - Gate40 Redbox attaches Local Area Network (LAN) or conventional Ethernet equipment to zero-delay recovery time Redundant Ethernet networks. All this network switching operations are managed by hardware ensuring high data throughput and reliability.

CPPS - Gate40 Redbox includes support for the latest IEEE1588-2008 version and profiles involved in the Substation Automation Systems enabling, as an example, the interconnection of IEEE1588-aware PRP networks with HSR ones.

CPPS - Gate40 Redbox consists of a modular embedded hardware and software system, powered by SMARTZynq module and by high-availability and synchronization IPs from **SoCe**. This technology is field proven and present in more than 15 countries worldwide.

In combination with **CPPS - Gate40 Sensor**, **CPPS - Gate40 Redbox** offers a powerful infrastructure that faces Cyber-Physical Production System requirements. It merges high computational capability, flexible and high availability industrial and IT networking, physical processing sensing and database management. This solution integrates different technologies and protocols to offer a Smart gateway platform which allows users to achieve accelerated business development into the IoT environment, merging the plant with the IT world.

Hardware Key Features

The "heart"' of the **CPPS - Gate40 Redbox** is a Xilinx Zynq device. This is the last generation of programmable System-on-Chip platforms. It embeds in the same device a double-core ARM-9 processor and a high-end FPGA section.

Communication interfaces:

- 4 SFP cages for 10/100/1000Base-Tx Ethernet copper, 100Base-FX and 1000Base-X fiber. These interfaces are driven by the FPGA section of the Zynq device providing low-latency switching capabilities. All switching implementations include an internal port that provides access to the network to the internal ARM9 multiprocessor.
- 1 10/100/1000Base-Tx Ethernet copper port directly attached to the internal ARM9 multiprocessor.

Memory features:

- 8 Gb DDR3: Fast DDR memory to store operating systems, software applications, protocols stacks or large buffers.
- 256 Mb Quad SPI Flash: Memory for firmware and bitstream storage.
- µSD connector: High density and low cost large storage for complex operating systems, permanent data storage and quick upgrade.
- EEPROM with unique MAC integrated: Ready to use unique MAC in each module to reduce the time-to-market of the customer product.

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Networking Key Features

SoCe IP cores provide on the FPGA section of the internal SoC chip flexible and powerful networking capabilities for both the Industrial and the IT Section. Tri-speed Legacy Ethernet ports can be combined with high availability "Plug&Work" Ethernet ports based on HSR and PRP zero-delay recovery time redundancy protocols. Among other switching configurations, it is worth to mention:

- 4x Legacy Ethernet ports.
- 2x HSR/PRP ports and 1 Legacy Ethernet port.
- 4x HSR/PRP ports.
- 2x HSR/PRP or Legacy ports and 2x Real Time Profinet ports.
- 2x HSR/PRP or Legacy ports and 2x Ethernet IP/DLR ports.

IEEE 1588 **SoCe** technology for sub-microsecond synchronization integrated on ***CPPS - Gate40 Redbox*** offers an "out-of-the-box" for IEEE 1588 implementations. The device can work as Master of the network, Slave and Boundary Clock. Furthermore, all **SoCe** switching implementations include Transparent-Clock functionality ensuring high precision synchronization in different and complex implementations.

Cyber-security Key Features

- Zynq-7000 Secure Boot, which provides private key cryptography (AES/HMAC) and public key cryptography (RSA) allowing sensitive software to be encrypted and authenticated in a chain of trust.
- IEEE 802.1X protocol, which provides an authentication mechanism to the devices wishing to attach to the network.
- MACsec standard, which defines a security infrastructure to provide data confidentiality, data integrity and data origin authentication.

Applications and Services

- IEC 62439-3 Clause 4 (PRP) and Clause 5 (HSR) compliant
- PRP/HSR Coupling, DAN (Doubly Attached Node) and QuadBox functions supported
- Synchronization: Hardware-based IEEE 1588v2 PTP Master/Slave/Boundary Clock supported
- SNTP to synchronize system clock in Internet

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Specifications

Network interfaces characteristics
4 SFP cages for 10/100/1000Base-Tx Ethernet copper or 1000Base-X fiber with LED indicators
1 10/100/1000Base-Tx Ethernet copper port with LED indicators
1 USB Female B type connector
Power Supply
supports input voltage range from 6V DC to 30V DC
Physical characteristics
Dimensions: 174 mm x 125 mm x 62 mm
Material: aluminium case with a tough plastic frame and interchangeable rubber brackets
Mounting: DIN rail wall mounting
Working temperature
-40 ºC to +85 ºC

Supported standards
IEC 62439-3 Clause 4 PRP "Parallel Redundancy Protocol"
IEC 62439-3 Clause 5 HSR "High-availability Seamless Redundancy"
IEEE 1588v2 PTP "Precision Time Protocol" Default, Power Profile and IEC 61850-9-3
IEEE 802.3 for 10Base-T
IEEE 802.3u for 100Base-TX
IEEE 802.z for 1000Base-X
IEEE 802.1Q for VLAN Tagging
IEEE 802.1D for STP (Spanning Tree Protocol)
IEEE 802.1w for RSTP (Rapid Spanning Tree Protocol)
IEEE 802.1Q for VLAN based Ethernet Priorities
IEEE 802.1p for Class of Service (CoS)
IEEE 802.1X access control for port based and MAC based authentication, MAC-Port binding and authentication for login security
IEEE 802.1ab for Link Layer Discovery Protocol (LLDP)
SNMP RFC 1157/RFC 3410
SNTP RFC 4330

Ordering information and contact

SoC*e*

System-on-Chip *engineering*, S.L.

C/Jose Maria Escuza 23 EDD
48013 - Bilbao (Bizkaia)
Spain

Phone: +34 944420700
E-mail: info@soc-e.com
Web: www.soc-e.com