UnmanagedEthernetSwitch IP Core

Full-crossbar IEEE 1588 Ethernet Switch in a single FPGA

General description

UnmanagedEthernet*Switch* IP core of **SoC***e* (**UE***S*) implements a *Plug-and-Play* Ethernet switch on reconfigurable devices. It does not require external configuration. It has been designed to address the maximum throughput using the minimum resources.

This switch implements a non-blocking crossbar matrix that allows wire-speed communication among all the ports. The switch buffers and verifies each frame before forwarding it. However the latency time has been minimized to nanoseconds order.

Furthermore, **UE***S* supports IEEE 1588 V2 Transparent Clock functionalities. This feature, that corrects PTP frames introducing the error generated by the switch, allows the interconnection of IEEE 1588 synchronized devices maintaining the highest levels of accuracy.

UE*S* is the perfect Ethernet Switch IP to implement Ethernet based Industrial Networks.

UE*S* can be used in combination with **SoC***e* **HSR-PRP***Switch* IP to introduce HSR and PRP capabilities in the ports that were required.

The combination of **UE***S* and **HSR-PRP***Switch* will offer the maximum performance and maximum compatibility with the standards.

UnmanagedEthernetSwitch IP key features

UE*S* IP core is:

- *High Performance*: Full-crossbar matrix among ports implemented to allow maximum throughput
- *Fast*: Very reduced Latency Times thanks to **SoC***e* proprietary MAC address matching mechanism
- *Efficient*: Optimized to require few logic resources in order to allow the implementation on low-cost FPGA devices
- *Plug-and-Play*: No configuration required
- *Flexible*: Fully scalable and configurable
  - Number of ports
  - MAC address Table Length
  - Buffers queue length
  - IEEE Transparent Clock functionalities
- *Extensible*: Zynq version available

Applications

UE*S* may be used in a wide range of products and applications. It offers a simple way to introduce Ethernet Switching capabilities IEEE 1588 aware.

- Industrial Networking
- Transportation

- Robotics
- Security
- Defense and Aerospace

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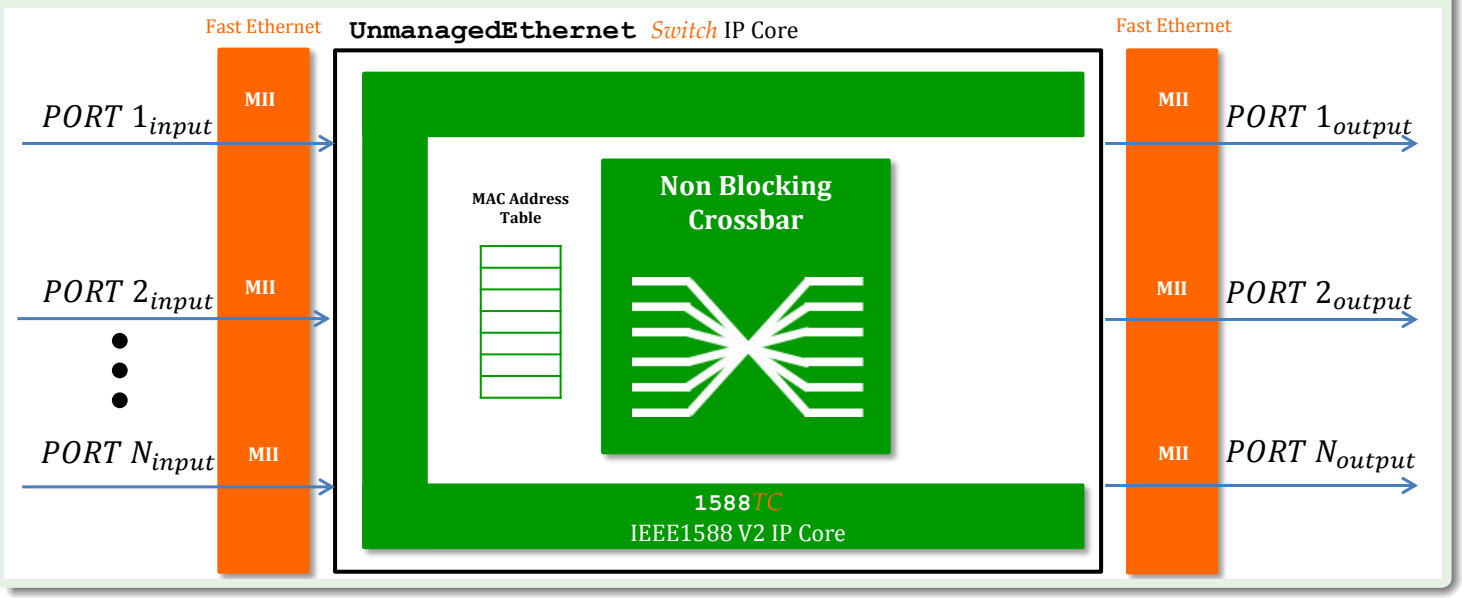
Block Diagram



Reference and Evaluation Designs

Features implemented on the Reference Designs:

- 4-port-switch (**NET***box*)
- Store capacity of 256 MAC addresses and 300 second aging time
- 32 frame store capacity and 16384 position x 8 bits buffer length in each port

Reference Designs and Evaluation boards:

- **NET***box* : Ready to download from **SoC***e* Web Site
- Xilinx SP605 Evaluation Board and ISM Networking FMC Module: Contact **SoC***e*
- Xilinx Zynq ZC702 Evaluation Board: Contact **SoC***e*

Ordering information and contact

SoC*e* offers for **UE***S* IP core the following licensing modes:

- 'One-shoot' encrypted VHDL source code - Site license
- 'One-shoot' encrypted VHDL source code (fixed number of ports) - Site license
- 'One-shoot' netlist - Project License

SoC*e*:
soceindustrial@soc-e.com
System-on-Chip *engineering*
48013 Bilbao SPAIN
Tlf: +34 944420700

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