

ManagedEthernetSwitch IP Core

Full-crossbar IEEE 1588 Managed Ethernet Switch in a single FPGA

General description

ManagedEthernetSwitch IP core of **SoCe (MES)** implements a configurable Ethernet switch on reconfigurable devices. It has been designed to address the maximum throughput using the minimum resources.

This switch implements a non-blocking crossbar matrix that allows wire-speed communication among all the ports. The switch buffers and verifies each frame before forwarding it.

It offers some configuration and statistic registers that are accessible via UART or AXI4-Lite interface.

Furthermore, **MES** supports IEEE 1588 V2 Transparent Clock functionalities. This feature, that corrects PTP frames introducing the delay caused by the switch, allows the interconnection of IEEE 1588 synchronized devices maintaining the highest levels of accuracy.

MES is the perfect Ethernet Switch IP to implement Ethernet based Industrial Networks. It supports 10/100/1000 Mbps Ethernet interfaces.



MES can be used in combination with **SoCe HSR-PRP Switch** IP to introduce HSR and PRP capabilities in the ports that were required.

The combination of **MES** and **HSR-PRP Switch** will offer the maximum performance and maximum compatibility with the standards.

ManagedEthernetSwitch IP key features

- *High Performance*: Full-crossbar matrix among ports implemented to allow maximum throughput
- *Efficient*: Optimized to require few logic resources in order to allow the implementation on low-cost FPGA devices
- *Port-based VLAN support*: switch can be virtually divided into virtual switches
- Address table with up to 2048 entries
- Possible to work with different data rate (10/100/1000 Mbps) for each port
- *Flexible*: Fully scalable and configurable
 - Number of ports
 - Buffers queue length
 - Configuration and statistic registers
 - IEEE Transparent Clock functionalities
- *Extensible*: Zynq version available

Applications

MES may be used in a wide range of products and applications. It offers a simple way to introduce Ethernet Switching capabilities IEEE 1588 aware.



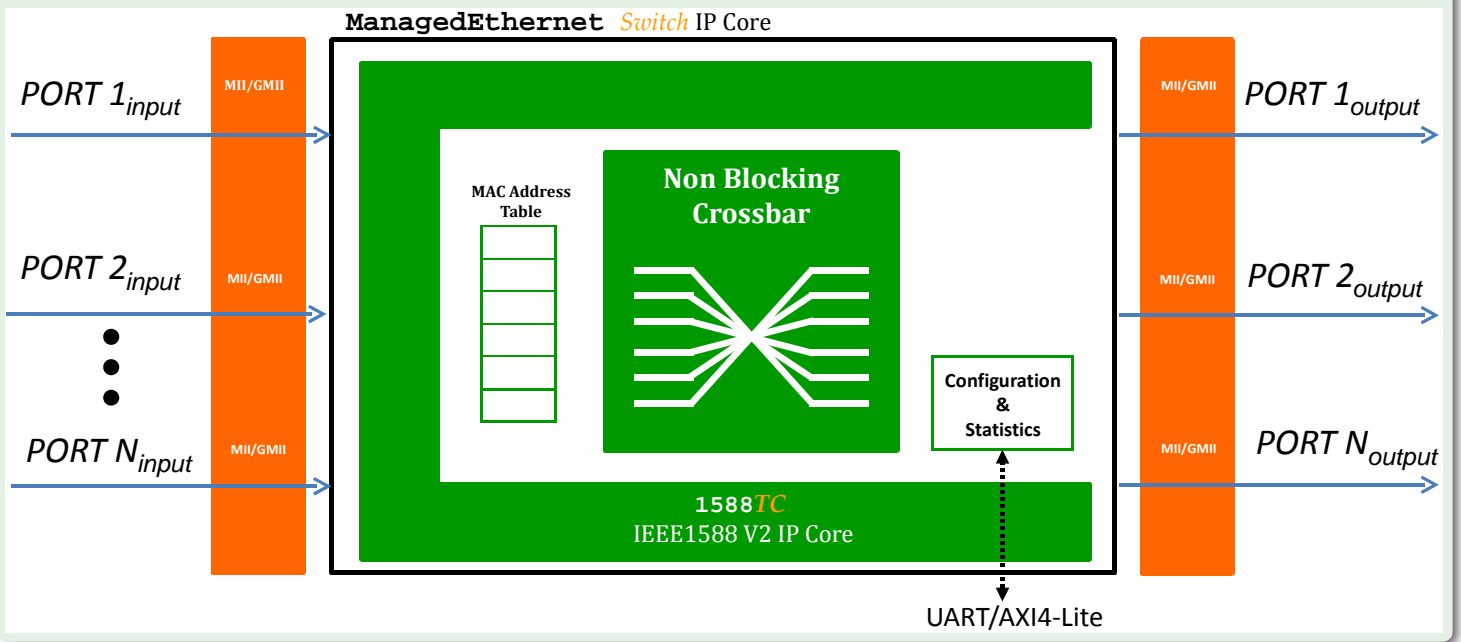
- Industrial Networking
- Transportation



- Robotics
- Security
- Defense and Aerospace



Block Diagram



Reference and Evaluation Designs

Features implemented on the Reference Designs:

- 4-port-switch
- Store capacity of up to 2048 MAC addresses
- UART or AXI4-Lite interface

Reference Designs and Evaluation boards:

- Xilinx SP605 Evaluation Board (up to 3 ports, 10/100/1000 Mbps): Contact **SoCe**
- Xilinx Zynq ZC702 Evaluation Board (up to 3 ports, 10/100/1000 Mbps): Contact **SoCe**

Ordering information and contact

SoCe offers for **ME S** IP core the following licensing modes:

- 'One-shoot' encrypted VHDL source code - Site license
- 'One-shoot' encrypted VHDL source code (fixed number of ports) - Site license
- 'One-shoot' netlist - Project License

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