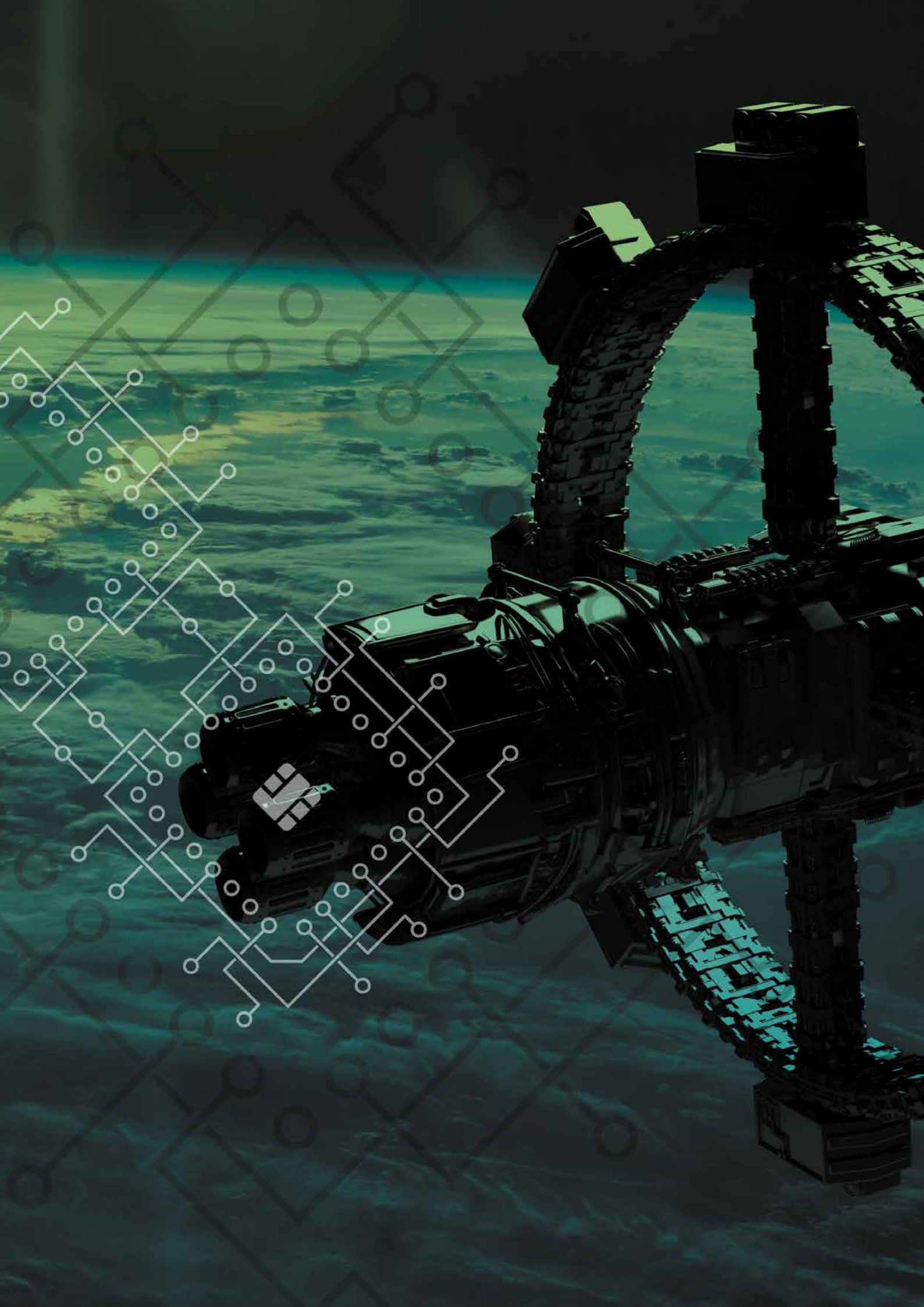
SoCe

System-on-Chip *engineering*

Timing, Networking & Security



Company Profile

Industry & Aerospace sectors demand solutions to simplify network implementation and operation. On the one hand, the amount of transmitted data grows dramatically, but on the other hand the standard solutions for Information Technologies (IT) do not match with the real-time operation requirements of these mission critical environments.

Ethernet has been identified as the ideal media interface to merge in a single network the real-time traffic required by Operational Technologies (OT) and the high volume of data demanded by the new applications located in the IT domain. The technologies required to make possible this integrated approach are: means for accurate synchronization, hardware implementations of time-triggered Ethernet and security solutions able to protect real-time traffic.

The next future is demanding more steps forward, and SoC-e is committed to support the latest innovation for its customers.

The SoC-e experience in these technologies has been applied in more than 100 projects worldwide and it has positioned SoC-e as a leader technology provider for time-aware high-availability Ethernet switching solutions.

The next future is demanding more steps forward, and SoC-e is committed to support the latest innovation for its customers. As an example, SoC-e is ready to provide a comprehensive solution for interoperable Time-Sensitive Networking and an ultra-low latency technology to secure the strict-real time traffic within Smart-Grid infrastructures.

We hope that the present catalogue works as a high level overview of what SoC-e can offer to speed up the integration of cutting-edge technology in your products. The new challenges of Industrial & Aerospace sectors invite us to be pioneers once again and we will be glad to share this vision with you.

The SoCe Team

Technology

Providing Time-Sensitive Networking

Industrial Internet of Things (IIoT) offers smarter infrastructure and hyper-connected devices with sensing, processing and networking capabilities. These systems will generate incredible amounts of data, sharing the same network. Thus, it is necessary to ensure that the real-time and critical-mission messages are transferred within strict bounds of latency and reliability regardless of other network traffic.

TSN stands for Time-Sensitive Networking. It is the name of the IEEE 802.1 Task Group responsible for standards at Data Link Layer. This group provides the specifications that will allow time-synchronized, low latency, streaming services through IEEE 802 networks. TSN is unique in that its streams are delivered with guaranteed bandwidth and deterministic latency.

Attending an information published by the analysts, the TSN market is expected to grow dramatically in the next five years, considering that most of the end-equipment will start being commercialized by 2019. Indeed, the first TSN capable end-equipments, like CISCO IE-4000 or some National Instruments modules have been launched to the market in 2018.

It is necessary to introduce TSN technology inside the hardware and software of its own products, because they will have an active role in the network.

However, for any company that forecast introducing TSN in their equipment it is not enough having access to third-party TSN switching equipment. It is necessary to introduce TSN technology inside the hardware and software of its own products, because they will have an active role in the network. This is a big challenge due to the diversity and complexity of the elements involved in the solution.

Thanks to the extensive field-proven experience on time-aware critical systems, SoC-e has released a comprehensive TSN solution thought to reduce the Time-to-Market and development risk to its customers. This solution has been designed to be implemented on programmable SoCs and it is available in different formats like IPs, ready-to-use modules or evaluation kits.

Providing High-Availability Networking

The demand for high-availability Ethernet has increased significantly last years. Electric, Defense and Industrial sectors are pushing for easy to implement IEC or IEEE standardized solutions.

SoC-e proposal for Reliable Ethernet is based on the IEC standards HSR and PRP combined with an accurate time synchronization layer provided by IEEE 1588 protocol. These interoperable protocols ensure zero-delay recovery time in case of a network failure and facilitate "Plus & Work" operation on critical mission scenarios.

SoC-e provides tailored high-availability switching solutions implementable on reconfigurable devices combining these optimized hardware blocks for HSR/PRP with logic for MRP, Managed Ethernet, field buses or with customer specific requirements.

SoC-e roadmap in this field goes beyond the state-of-the-art and presents in this catalog innovative implementations for Deterministic HSR and for Secure HSR in order to fulfill the most demanding requirements that will arise in critical-mission applications.

Providing Security for Critical-Mission Embedded Systems

Cybersecurity is a huge challenge for Industry and for Critical Systems in general. A multi-layered approach is mandatory to cover the security threats that may arise at sensor, electronic device, embedded device, application, OT/IT networks and Cloud levels. Therefore, the number of required solutions involved is large and the technologies to apply are very heterogeneous.

SoC-e is aware of this reality and it is focused on providing solutions for sectors that demand on-the-fly protection mechanisms for real-time traffic and trusted platforms.

As a result of this strategy, SoC-e has developed in-house a wire-speed cryptographic solution. It is integrated in the new IPs for secure high-availability Ethernet networking and for Substation Automation Systems control traffic protection.

In order to offer more comprehensive security solutions, SoC-e has completed its product portfolio with a software package to implement network and application level security on embedded systems and with a software stack that implements security keys and certificates exchange mechanism as it is being defined by IEC.

IP Cores for FPGAs

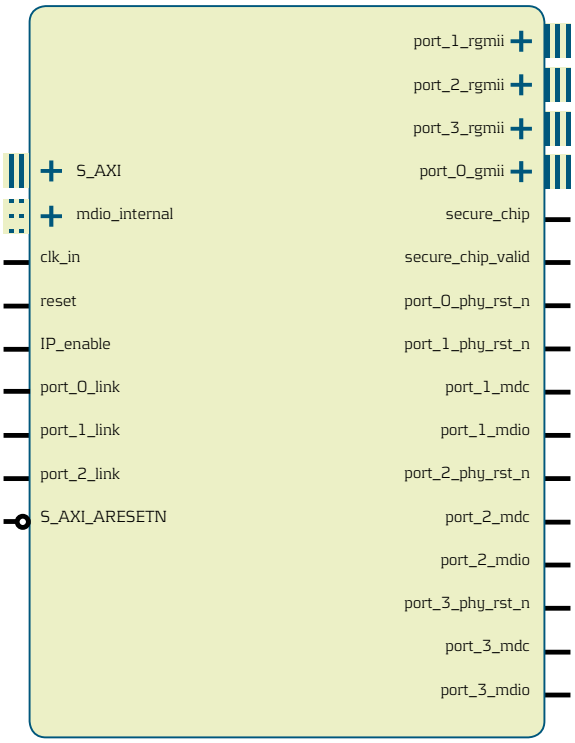
Deterministic Ethernet Switch IPs

Multiport TSN Switch IP

Time-Sensitive Networking (TSN) is an IEEE standardized solution that merges Real-Time traffic with Best-Effort one in a single Ethernet Network. TSN ensures delivering streams with guaranteed bandwidth and deterministic latency.

SoC-e's TSN solution is called Multiport-TSN Switch (MTSN) IP. It can be implemented optimally depending on the requirements of the final product, from a simple 2-port unit to a complex multiport switch. This IP has been designed to be implemented on Programmable SoCs. As an example, targeted devices are the Xilinx Zynq Ultrascale+ MPSoC. Therefore, the IP includes Hardware and Software packages.

The designer can select, among other parameters, the number of ports and memory distribution for the switch implemented in the FPGA section. This entire configuration is done graphically in Xilinx Vivado Tool.



MTSN_Switch*

Key Features:

- Non-blocking matrix architecture: 100% data throughput for GbE traffic
- Up-to 16 ports
- Traffic Type Supported: Scheduled traffic, Best-effort Traffic and Reserved Traffic
- Time Aware Shaper: Configurable number and size of time slots
- Credit Based Shaper: Configurable bandwidth reservation for each traffic class
- Full-duplex 10/100/1000 Mbps Ethernet Interfaces
- Full-duplex 10 Gbps Ethernet Interfaces for standard Ethernet ports
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X
- Xilinx 7-Series and Ultrascale/ Ultrascale+ devices supported
- IEEE 802.1 AS(rev) for Time Synchronization Layer
- IEEE 802.1 Qbv, Qcc, Qci*, QCB*
- Jumbo Frame Management
- Broadcast Storm Protection
- Port-based VLAN support
- Reference Designs and Evaluation Kits available

*__Note:__ As the IPs are configurable, all IP blocks represented in this catalog may include only a subset of the total signals present in the IP

IP Cores for FPGAs

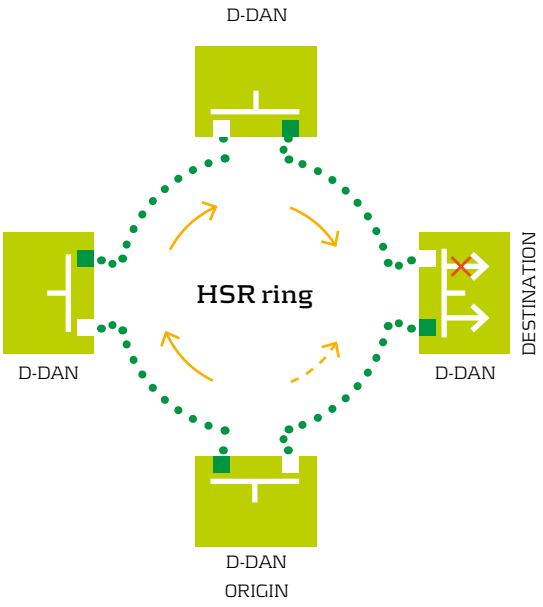
Deterministic HSR IP

High-availability Seamless Redundancy (HSR, IEC 62439-3-Clause 5) provides redundancy by sending packets in both directions through a ring networkIn case of an interruption in the ring,, a HSR capable destination node always receives the frames through one other port.

The standard defines priority for the traffic received from the ring. Therefore, it is feasible calculating the worst case scenario for the delivery of a message within a HSR ring. This behavioral allows using standard HSR in some real-time environments.

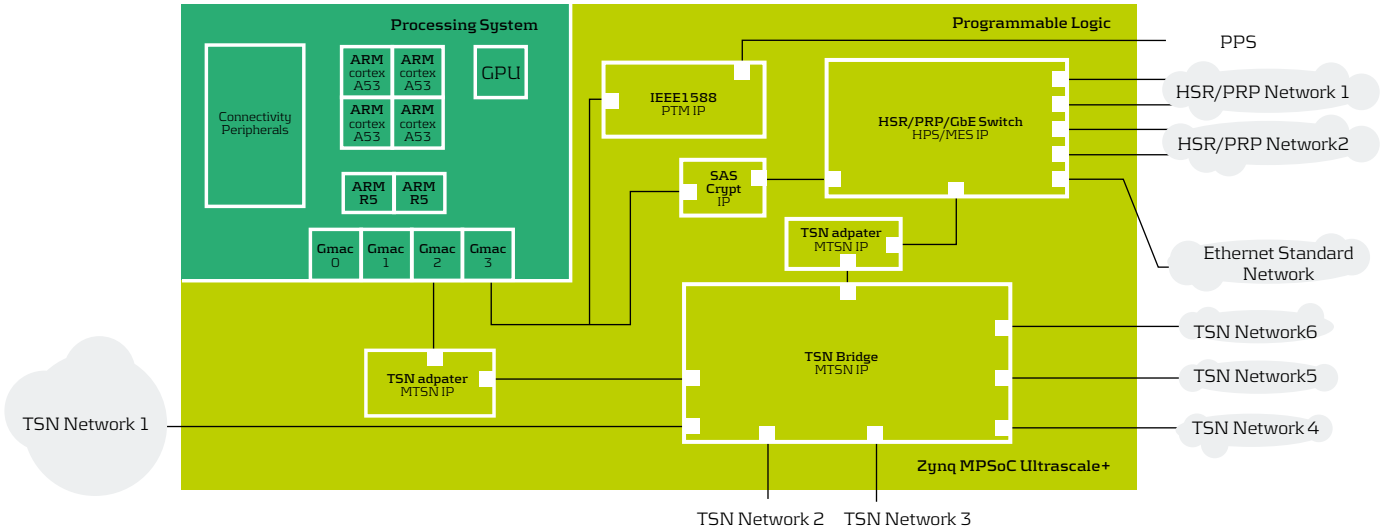
However, if the timing and bandwidth use restrictions are severe, it is necessary adding a timing plane to the HSR nodes in order to deliver the data traffic in an scheduled way. IEEE 1588 protocol is the driver to build a deterministic HSR solution focused on rugged sectors like Electric or Defense that prefers a robust hardware based solution simpler than the general purpose TSN one.

Deterministic HSR (D-HSR) is a hardware based solution optimized for reconfigurable devices ready for being upgrade if IEC releases a final inter-operable standard.



General Key Features

- Deterministic precise frame sending in HSR
- Cyclic time-division multiplexing based on precise clock synchronization
- Shares the general features listed for
- HSR/PRP Switch IP product



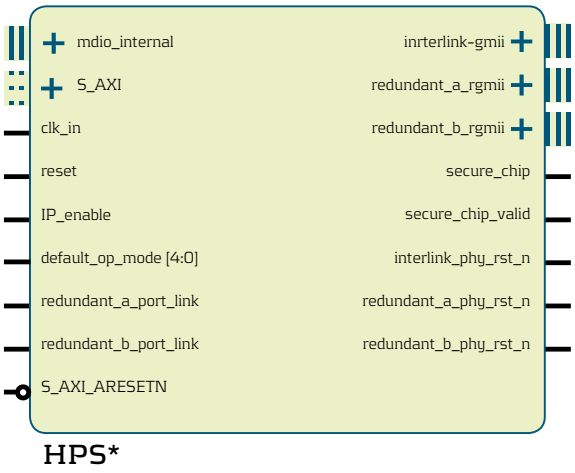
IP Cores for FPGAs

High-Availability Ethernet Switch IPs

HSR/PRP Switch IP

This IP implements bumpless Ethernet connectivity ensuring zero-delay recovery time in case of network failure and no-frame lost. The IP supports the latest version of High-availability Seamless Redundancy (HSR) and Parallel Redundancy Protocol (PRP) standards in combination with redundant IEEE 1588-2008. The flexibility and scalability of this IP offer optimized solutions for cost-sensitive CPU-less equipments and for high-end complex MPSoC based networking platforms.

Each HSR/PRP port pair is implemented with a dedicated hardware module. These modules can be easily combined with the Managed Ethernet Switch IP to implement multiport and heterogeneous switches that mixes standard and high-availability ports.



Key Features

- IEC 62439-3 (clauses 4-5) v3
- Up-to 16 ports
- IEEE1588-2008 support
- Optimized architecture to avoid HOL effect
- Cut-through and Store & Forward combined switching architecture
- Full-duplex 10/100/1000 Mbps Ethernet Interfaces
- Full-duplex 10 Gbps Ethernet Interfaces for standard Ethernet ports
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X
- Supervision Frames and IEEE 1588v2 Transparent Clock operation processed by hardware
- CPU-less version available
- Distributed memory architecture for maximum reliability and scalability
- Traffic segregation based on Ethernet Type with dedicated memory buffers support
- QoS based on Priorities (PCP-802.1p, DSCP TOS)
- QoS based on Ethernet Frames Types
- IEEE 1588v2 Stateless Transparent Clock functionality
- Security IEEE 802.1X and EAPOL hardware support
- MDIO, UART, AXI4-lite or Configuration-over-Ethernet (CoE) management interfaces
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ devices supported
- Reference Designs and kits available (SMARToem, SMARTmpsoc, SMARTzynq)

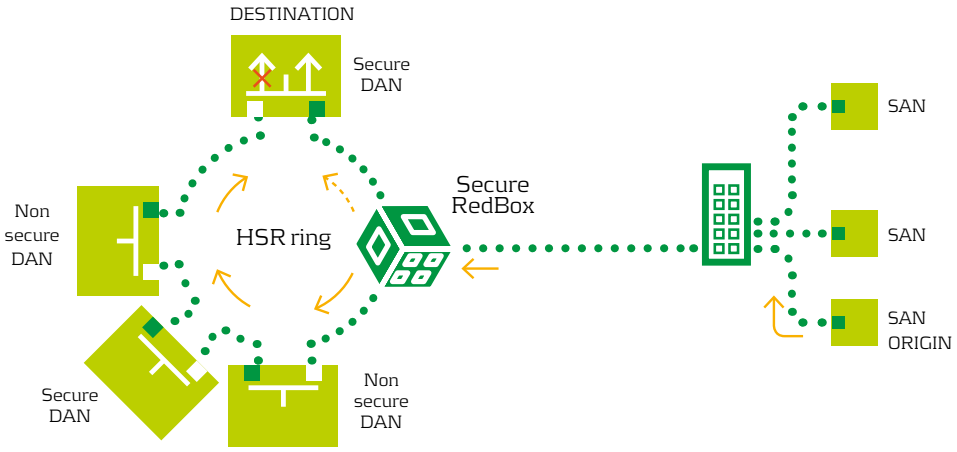
IP Cores for FPGAs

Secure HSR Switch IP

High-availability Seamless Redundancy (HSR, IEC 62439-3-Clause 5) is an IEC standard that is gaining acceptance for control-related network rings. As an example, it is used for process bus in substations, for Ethernet backbones in military vehicles or for train signaling control.

In these critical scenarios, advanced means for security are demanded. The authenticity of the data needs to be ensured and in some cases, the confidentiality is also desired.

SoC-e proposes a Secure HSR (S-HSR) solution that comprises a low-latency cryptographic implementation that allows simultaneous encryption and authentication.



S-HSR frame format has been designed in order to ensure interoperability with standard HSR nodes. This feature facilitates the introduction of secure HSR equipment gradually.

Key Features

- Interoperable with HSR legacy equipment
- No added latency in mid HSR boxes
- Cut-through operation feasible
- Both encryption and authentication supported
- Shares the general features listed for HSR/PRP Switch IP product

MRP Switch IP

Media Redundancy Protocol (MRP) is a data network protocol standardized by the International Electrotechnical Commission (IEC) as IEC 62439-2. MRP allows rings of Ethernet switches to overcome any single failure with recovery time much faster than achievable with traditional alternatives like Spanning Tree Protocol. However, it is not able to offer zero-delay recovery time like PRP or HSR. it is suitable to most Industrial Ethernet applications and it is quite popular in some sectors.

MRP Switch IP supports the role of client (Media Redundancy Client - MRC) or manager (Media Redundancy Manager - MRM). These modes of operation are fully implemented on hardware, and there is no need for MRP software stack.

Key Features

- MRP hardware processing
- Media Ring Manager (MRM) supported
- Media Ring Client (MRC) supported
  - Non-blocking matrix architecture: 100% data throughput for GbE traffic
  - Up-to 16 ports
  - Optimized architecture to avoid HOL effect
  - Full-duplex 10/100/1000 Mbps Ethernet Interfaces
  - Half-duplex 10/100 Mbps Ethernet Interfaces
  - MII/RMII/GMII/RGMII/SGMII Physical Layer device (PHY) interfaces
  - Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X
  - IEEE 1588-2008 P2P/E2E Transparent Clock operation run by hardware
  - Jumbo Frames
  - Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/Ultrascale+ devices supported

IP Cores for FPGAs

Time-aware & Industrial Ethernet Switch IPs

The integration of Ethernet Switches on FPGA is simplifying the communication between heterogeneous systems and applications. Thanks to the flexibility of reconfigurable devices combined with networking IPs, the end-equipment embeds not only Ethernet endpoint capabilities but added-value switching features as well. In addition, the low switching latency of SoC-e IPs implemented over a non-blocking matrix infrastructure is a robust base for networking in critical systems. As an example IEEE 1588-2008 support or storm protection means are fully implemented in hardware. This flexible architecture ensures port number scalability and simplifies the integration of the IP in the systems. SoC-e has developed a portfolio of Ethernet Switching IPs focused on different applications and sectors. Therefore, it is feasible combining the features of different IPs to obtain finally an optimal solution for each case.

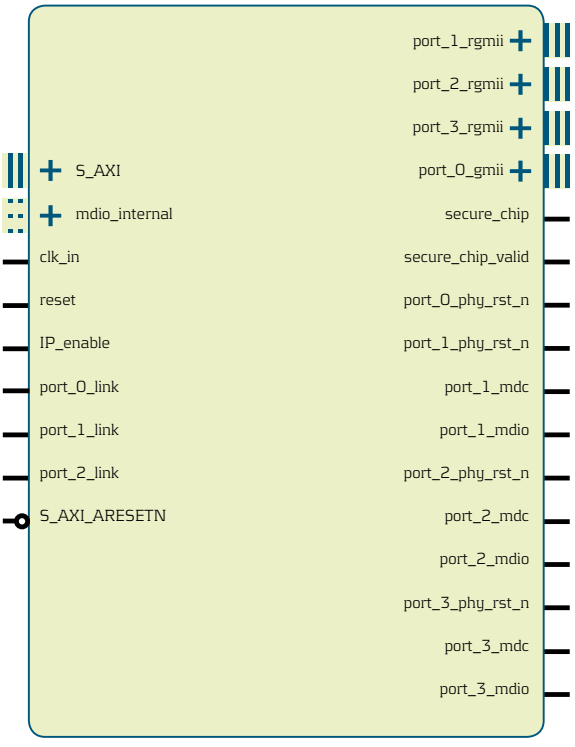
Ethernet Switch IPs General Key Features

- Non-blocking matrix architecture: 100% data throughput for GbE traffic
- Up-to 16 ports
- Optimized architecture to avoid HOL effect
- Full-duplex 10/100/1000 Mbps Ethernet Interfaces
- Half-duplex 10/100 Mbps Ethernet Interfaces
- Full-duplex 10 Gbps Ethernet Interfaces
- MII/RMII/GMII/RGMII/SGMII/QSGMII Physical Layer device (PHY) interfaces
- Copper and Fiber-optic media interfaces: 10/100/1000Base-T, 100Base-FX, 1000Base-X
- IEEE 1588-2008 P2P/E2E Transparent Clock operation run by hardware
- Jumbo Frames
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/Ultrascale+ devices supported
- Reference Designs and kits available (SMARTmpsoc, SMARTzynq)

Managed Ethernet Switch IP

Specific Key Features

- Managed Ethernet Switch IP
- Distributed Switch Architecture (DSA) support
- QoS based on Priorities (PCP-802.1p, DSCP TOS)
- QoS based on Ethernet Frames Types
- Port-based VLAN switching
- EtherType Based switching
- Multicast Frame Filtering
- Broadcast & Multicast Storm Protection
- Per-Port Rate limiting (Broadcast, Multicast and Unicast traffic)
- Switching Portmask: User-defined forwarding of frames to defined ports
- IEEE 1588v2 Stateless Transparent Clock functionality (P2P/ E2E)
- Security IEEE 802.1X and EAPOL hardware support
- Hardware support for RSTP
- MDIO, UART, AXI4-lite or Configuration-over-Ethernet (CoE) management interfaces



MES*

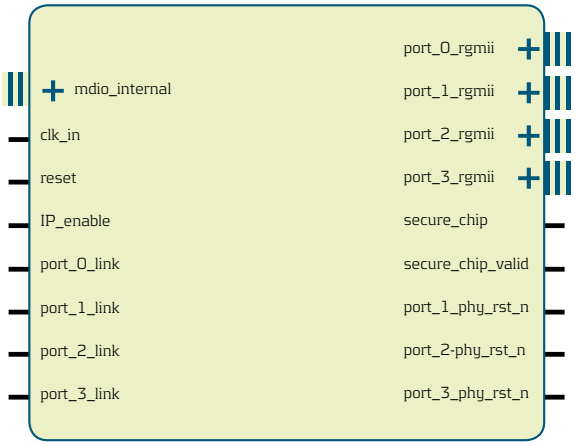
IP Cores for FPGAs

Unmanaged Ethernet Switch IP

Specific Key Features:

- Plug&Work operation
- Optimized for maximum performance with minimal FPGA resources

Cyber-Security Surveillance



UES*

Switch IP

Key Features:

- Port mirroring for aggregated selected ports
- Traffic classification attending traffic type (different queues) Zynq/MPSoC references design under Linux (SMARTzynq/SMARTmpsoc boards)
- Non-intrusive hardware support for Network Intrusion Detection Systems (NIDS)

Ethernet IP/DLR IP

Specific Key Features:

- Multiport support combined with DLR port pair
- DLR management supported by hardware by port pairs.
- Beacon Based Node
- Supervisor Node
- CPU-less Beacon processing

Profinet IP

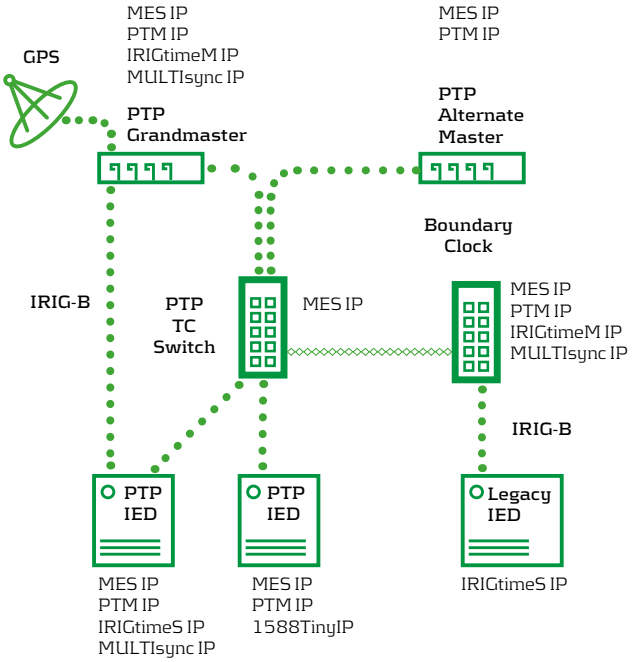
- Specific Key Features:
- Profinet RT CC-B Line Structure supported
- Multiport support

IP Cores for FPGAs

MULTIsync IP

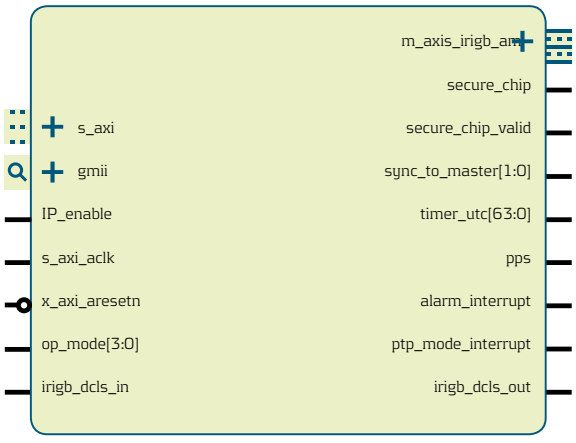
MULTIsync IP Core is a multi-protocol, redundant time synchronization core that provides sub-microsecond time synchronization, providing maximum flexibility for every scenario. It is able to achieve accurate time synchronization using IEEE 1588-2008 (PTPv2) and IRIG-B time protocols. This versatility enables different cases-of-use that are complementary:

- Clocking source redundancy: It is feasible connecting the IP to a PTP network and to an IRIG-B master at the same time. The user selects which is the time source used between the three available (PTP, IRIG-B, free running timer)
- Clocking Bridge: It runs as a PTP to IRIG-B or IRIG-B to PTP bridge while the IP is synchronized with the selected master
- Clock Master Functionality: It can act a PTP or IRIG-B master



Key Features

- IRIG 200-04 compliant time synchronization master and slave
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Output type (IRIG-B timecode) configurable both before implementation and on-the-fly
- IEEE 1588v2 Profiles supported:
  - Default
  - Power
  - Power-Utility (IEC61850-90-3)
  - 802.1AS
- Upgradeable to IEEE1588v2.1/v3 and to 802.1ASrev
- Synchronization input (slave) sources:
  - PTP: Ethernet. PTP Slave at the input
  - IRIG-B: IRIG-B compliant signal. IRIG-B Slave at the input
  - Free Running Timer: Digital input
- Synchronization output (master) options:
  - PTP: Ethernet. PTP master at the output
  - IRIG-B: IRIG-B compliant signal. IRIG-B Slave at the output
  - Free Running Timer: Digital Output
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ devices supported



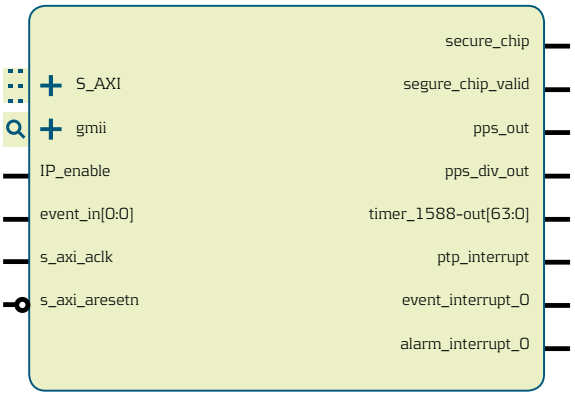
MULTIsync*

IEEE 1588 Precise Time Multi-profile IP

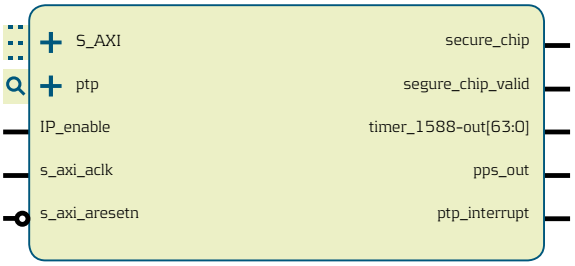
The integration of this IP in your design provides an outstanding synchronization mechanism that only requires Ethernet connection to obtain nanosecond range synchronized timers in your equipment. This IP is capable of accurately time stamp IEEE 1588 telegrams and it also embeds the timer and auxiliary signals. All these processes are carried out by hardware modules. The IP is delivered with all the necessary software to run under any Xilinx reconfigurable platform.

Key Features:

- Hardware and software to support Ordinary , Transparent and Boundary Clock functionalities
- GMII or AXI-4 selectable interfaces to support:
  - » Full-duplex 10/100/1000 Mbps Ethernet
  - » Half-duplex 10/100 Mbps Ethernet
  - » Full-duplex 10 Gbps Ethernet
- 32 bit seconds / 32 bit nanoseconds counter
- 32 bit sub-nanosecond frequency adjust
- Pulse Per Second (PPS) Output available
- Frequency Selectable Output available (1 KHz/2 KHz/4 KHz/8 KHz/16 KHz/32 KHz)
- IRIG-B Master Output
- PTP on both Layer 2 (Ethernet) and Layer 3 (IPv4) interfaces supported
- Seamless integration with HSR-PRP and Ethernet switch IP cores
- VLAN support
- IEEE 1588v2 Profiles supported:
  - » Default
  - » Power
  - » Power-Utility (IEC61850-90-3)
  - » 802.1AS
- Upgradeable to IEEE1588v2.1/v3 and to 802.1ASrev
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ devices supported



PTM*

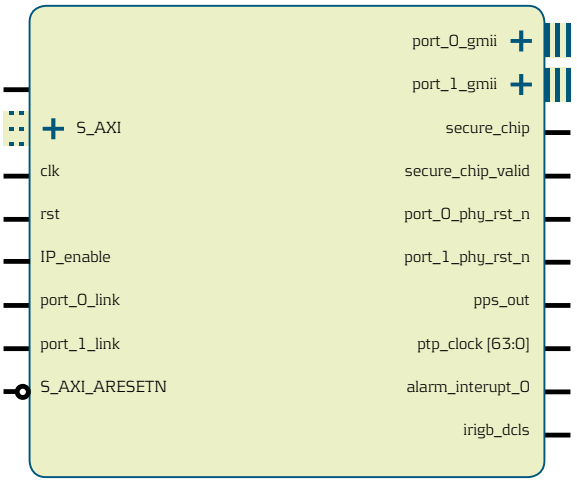


PTM Lite*

IP Cores for FPGAs

1588Tiny Slave-Only IP

This IP offers the simplest solution available in the market to integrate IEEE 1588-2008 slave capabilities to any equipment. 1588Tiny embeds the Ethernet MAC, parsing and timestamping units, and the computation logic required to output a synchronized clock and a PPS output. This IEEE1588v2 Slave Only hard-only compliant clock synchronization IP core is focused on equipments that require basic IEEE 1588 functionality using the minimum resources and complexity. Therefore, 1588Tiny does not require any software, it can run in CPU-less boards and it can be embedded also with HSR-PRP and Ethernet IP Switch IP cores that provide hardware supported Transparent Clock operation.

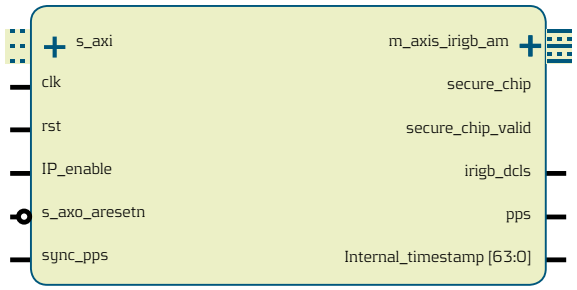


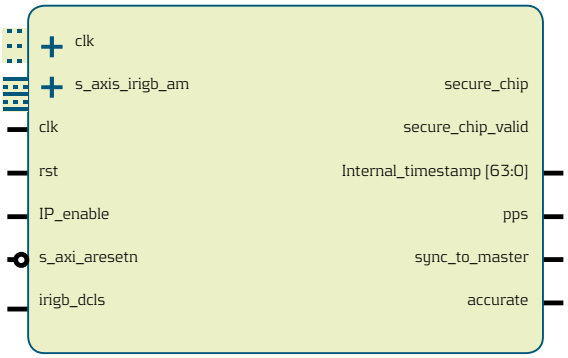
1588_Tiny*

Key Features:

- CPU-less operation (no software required)
- IEEE 1588v2 slave -only operation
- 64 bit Timer value available to customer logic
- Embedded Ethernet interfaces to support:
  - Full-duplex 10/100/1000 Mbps
  - Half-duplex 10/100 Mbps
- Full-duplex 10 Gbps support through AXI4 interface
- PPS output signal
- Optional IRIG-B Master Output
- IEEE 1588v2 Profiles supported:
  - Default
  - Power
  - Power-Utility (IEC61850-90-3)
  - 802.1AS
- Upgradeable to IEEE1588V2.1/v3 and to 802.1ASrev
- Xilinx Spartan-6/Virtex-6, 7-Series and Ultrascale/ Ultrascale+ devices supported

IP Cores for FPGAs





IRIG-B Master IP

This IP implements an IRIG 200-04 compliant time synchronization master on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations providing the maximum flexibility and accuracy.

Key Features:

- IRIG 200-04 compliant time synchronization master
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Output type (IRIG-B timecode) configurable both before implementation and on-the-fly
- Precise IRIG-B output in order to provide nanoseconds precision
- 32-bit timestamp input for initial set up of the IP
- Periodic pulse output for testing
- Autonomous operation by hardware

IRIG-B Slave IP

This IP implements an IRIG 200-04 compliant time synchronization slave on FPGA devices. It has been designed to support all the IRIG-B coded expressions as well as DCLS and AM modulations in order to provide maximum flexibility, accuracy and autonomy.

Key Features:

- IRIG 200-04 compliant time synchronization slave
- Support for DCLS and AM modulations
- Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
- Sub-microsecond synchronization with the IRIG-B master
- 64-bit internal timer synchronized in time and frequency with the IRIG-B master
- 32-bit for timestamp in seconds and 32-bit for nanoseconds
- Periodic pulse output for testing
- Autonomous operation by hardware

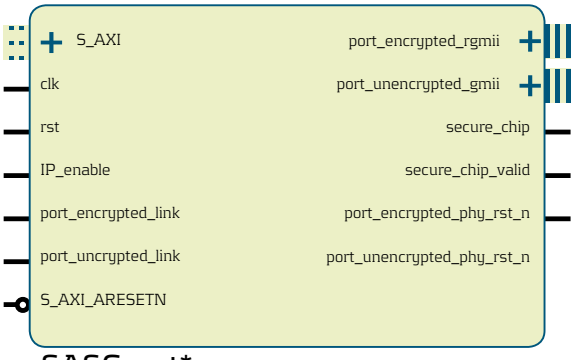
IP Cores for FPGAs

Substation Automation Systems Crypto-core IP

This IP faces the challenge of securing the most time-critical control messages in SAS and Smart-Grid: GOOSE and Sample Measured Values. The new generation of equipment for these specialized sectors needs to offer the highest level of reliability and security. Thanks to this IP, it is feasible implementing the most exigent security standards ensuring the strict response time defined in the IEC 61850 standard.

Key Features:

- GOOSE & SVM secured frame format support (IEC 62351-6, optional IEC 61850-90-5)
- Cipher and decipher operation
- AES-GCM cipher suite
- Wire speed operation
- Minimum latency time for tightly real time constrained GOOSE and SVM messages
- Designer selectable latency/throughput/FPGA resources trade-off
- Key management according to IEC 62351-9
- Combinable with SoCe networking IPs



SASCrypt*

Secure Configuration-over-Ethernet IP

SoC-e has developed a Layer-2 Ethernet based configuration protocol to access to FPGA systems named Configuration-over-Ethernet (CoE). CoE is useful to access the FPGA from off-board CPUs or SCADA/PC systems using Ethernet data link. Secure Configuration-over-Ethernet IP is a new edition of this IP that supports secured CoE frames to allow the use of this protocol on open networks.

Key Features:

- Configuration and control protocol over Ethernet between external CPU or SCADA/PC and the FPGA
- AES-GCM secured
- Reduced FPGA resources utilization
- Software API and program examples provided for the CPU or PC system

IP Cores for FPGAs

Secure IEEE 1588

SoC-e proposes a secure IEEE 1588 implementation for accurate time distribution. It is based on Layer-2 MACSEC security and ensures protection for one of the most difficult protocols to secure, the Precise-Time-Protocol (PTP).

This security solution is ideal for private and specialized networks where time accuracy is crucial like in Aerospace, Defense and Electric sectors. This protection added to IEEE 1588 traffic has been tested in real scenarios showing no impact on the achieved accuracy level.

The Security Key distribution challenge can be addressed using any standard Key Distribution scheme used in IT Networks or sector specific ones, like the IEC 62351-9 standard for Security Ket Management defined for the Electric sector.

Key Features:

- PTP Ordinary Clock and Boundary Clock support
- Based on MACSEC security
- Seamless integrable on Reconfigurable SoC Platforms
- Different alternatives for Security Key Management

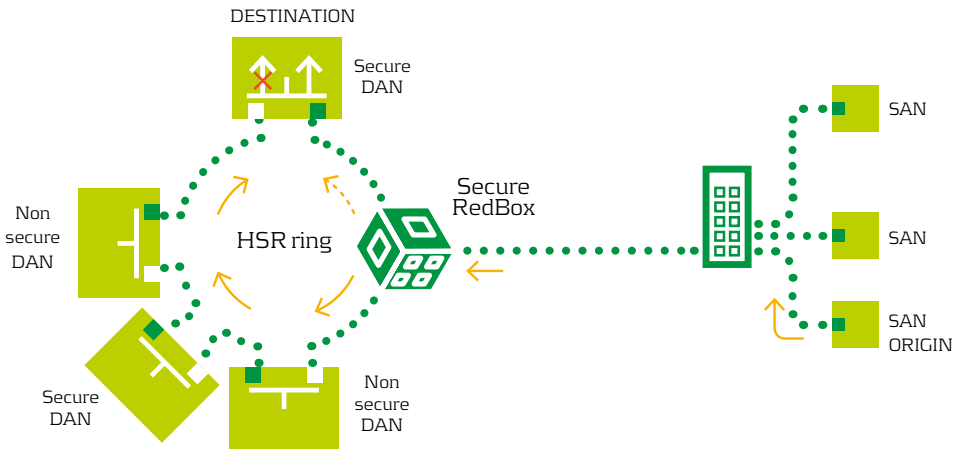
Secure HSR IP

High-availability Seamless Redundancy (HSR, IEC 62439-3-Clause 5) is an IEC standard that is gaining acceptance for control-related network rings. As an example, it is used for process bus in substations, for Ethernet backbones in military vehicles or for train signaling control.

- In these critical scenarios, advanced means for security are demanded. The authenticity of the data needs to be ensured and in some cases, the confidentiality is also desired.
- SoC-e proposes a Secure HSR (S-HSR) solution that comprises a low-latency cryptographic implementation that allows simultaneous encryption and authentication. S-HSR frame format has been designed in order to ensure interoperability with standard HSR nodes. This feature facilitates the introduction of secure HSR equipment gradually.

Key Features:

- Interoperable with HSR legacy equipment
- No added latency in mid HSR boxes
- Cut-through operation feasible
- Both encryption and authentication supported
- Shares the general features listed for HSR/PRP Switch IP product



FPGAs

SMARTmpsoc Family

New generation System-on-Chip devices embed heterogeneous CPU to address optimum Edge computing services. SoC-e has designed SMARTmpsoc, a pluggable System-on-Module (SoM) to simplify the integration of custom networking and synchronization capabilities combined with these powerful heterogeneous CPU architectures.

The heart of this SoM is a long term supply Xilinx Zynq MPSoC Ultrascale+ reconfigurable platform device that includes 6 ARM processors, a GPU and a high-end FPGA in a single device. The module is completed with industrial grade Gigabit Ethernet Phys, SATA-3 connector for high-capacity data storage unit, dedicated integrated circuit for security functions and RAM and Flash memory devices.

Module

Key Features

- Xilinx Zynq MPSoC Ultrascale+ XCZU3EG-SFVA625-1-I
- Optional XCZU2EG device
- Rugged for industrial applications
- Heterogeneous CPUs in a single IC:
  - 4x ARM Cortex-A53 CPU
  - 2x Dual-core ARM Cortex-R5 CPUs,
  - 1x Mali™-400 MP2 GPU
  - High-end Ultrascale+ FPGA
- 5x Ethernet Phys 10/100/1000BaseT-X
- 3x PS-GTR Transceivers
- 2 GB DDR4 RAM memory
- 64 MB Quad SPI Flash Memory
- 16GB eMCC Flash memory
- Battery for Real Time Clock (RTC)
- Trusted Platform Module (TPM) 1.2/2.0 security Chip.
- SATA-3 Connector
- Footprint compatible with SMARTzynq and SMARToem SoMs
- Size: 88x66 mm

Applications

- Edge computing device with advanced Ethernet networking capabilities
- TSN endpoint nodes and bridges
- Managed HSR/PRP/Ethernet embedded switch
- Synchronization device (Full IEEE 1588-2008 support)
- Network SoM for critical-mission applications
- Cybersecurity appliance: IDS, SIEM agents, on-the-fly encryption, etc.
- Software Defined Networks

Extendend brick

Key Features:

- Standard Brick Functionalities plus:
- USB Support
- Connection to 3x PS-GTR transceivers supporting:
  - SGMII connectivity
  - High-speed connectivity standards

Brick

Key Features

- 4x SFP cages for 10/100/1000Base-T, 100Base-FX or 1000Base-X
- 1x RJ45 for 10/100/1000BaseT
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

Kits

1588-aware HSR/PRP/Ethernet Switch Module

MTSN Kit: a Comprehensive Multiport TSN Setup

FPGAs

SMARTzynq Family

The heart of the SMARTzynq family is a pluggable System-on-Module (SoM) designed to enable easy integration of specialized Gigabit Ethernet switches in smart equipment for Electric, Industrial and Aerospace sectors. The Zynq programmable SoC platform embedded in the board includes a high-end FPGA and a dual core ARM9 CPU able to drive 5 tri-speed ports combining hardware IPs and software processing.

Applications:

- Managed HSR/PRP/Ethernet embedded switch
- IEEE 1588-2008 Master, Slave and Boundary Clock equipment
- Out-of-the-box embedded CPU solution
- TSN endpoint nodes and bridges
- Smart gateways for heterogeneous networks interconnection
- Advanced Cybersecurity applications: NDIS, SIEM agents, on-the-fly encryption, etc.

Module:

Key Features:

- Xilinx Zynq Programmable SoC XC7Z7010-7020
- Rugged for industrial applications
- Double core 32 bit ARM Cortex-A9
- 5x Ethernet Phys 10/100/1000BaseT-X
- 8 Gb DDR3 RAM memory
- 256Mb QSPI Flash memory
- uSD card memory
- Size: 88x60mm

Brick

Key features:

- 4x SFP cages for 10/100/1000Base-T, 100Base-FX or 1000Base-X
- 1x RJ45 for 10/100/1000BaseT
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD

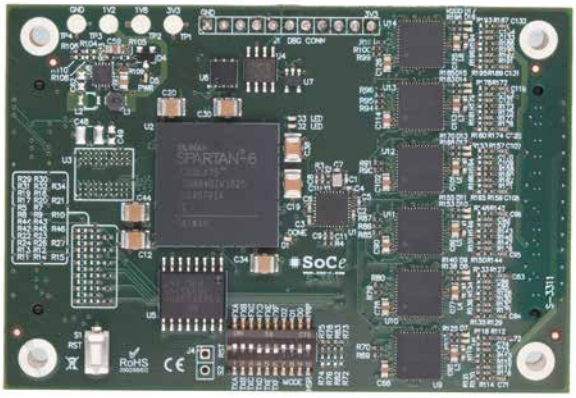
Kits

1588-aware HSR/PRP/Ethernet Switch Module

MTSN Kit: a Comprehensive Multiport TSN Setup

FPGAs

SMARToem Family



SMARToem family enables easy integration of added-value Ethernet Networks in equipment for Electric, Industrial and Aerospace sectors. The heart of the system is a Spartan-6 Xilinx FPGA able to drive up-to 6 Fast Ethernet ports or an 7-Series FPGA connected totri-speed Ethernet Phys . The module can be used to implement a user defined design or can be purchased with any of the SoC-e Networking and synchronization IPs.

Applications:

- HSR/PRP/Ethernet embedded switch
- 1588-aware switches
- Hybrid Clock devices for distributed sensor acquisition
- Custom Ethernet switch
- Industrial Ethernet gateways
- Cybersecurity applications

Spartan-6 Module

Key Features:

- Scalable Spartan-6 Xilinx FPGA LX45-LX150
- Rugged for industrial applications
- 6x Ethernet Phys 10/100BaseT-100BaseFX
- Support for Dynamic Bitstream Configuration (DBC)
- Support for Configuration-over-Ethernet (COE)
- Optional 512 Mb LPDDR
- 128 Mb Quad SPI Flash: Memory for Firmware and bitstream storage
- EEPROM with unique MAC address
- Embedded Temperature Sensor

Spartan-6 Brick

Key Features:

- SMARToem module
- Carrier for SMARToem module
- 3x SFP cages for 100Base-FX
- 3x RJ45 for 100Base-TX
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

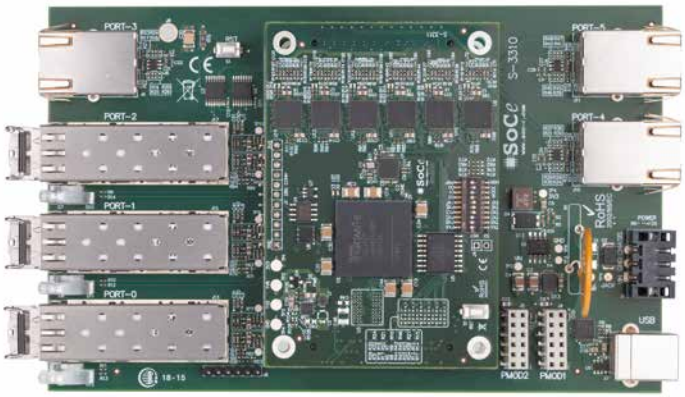
Spartan-6 Kit:

- 1588-aware HSR/PRP/Ethernet Switch Module

7-Series Module

Key Features:

- Scalable 7-Series Xilinx FPGA
- Rugged for industrial applications
- Multiple Ethernet Phys: 10/100/1000Base-T, 100Base-FX, 1000Base-X
- Support for Dynamic Bitstream Configuration (DBC)
- Support for Configuration-over-Ethernet (COE)
- Quad SPI Flash: Memory for Firmware and bitstream storage
- EEPROM with unique MAC address
- Embedded Temperature Sensor



7-Series Brick:

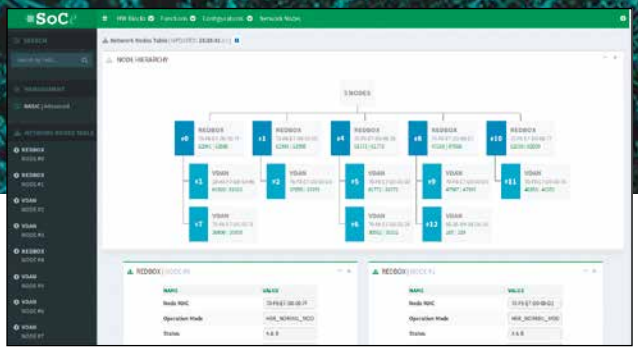
Key Features:

- 7-Series SMARToem module
- Carrier for 7-Series SMARToem module
- SFP cages for 10/100/1000Base-T, 100Base-FX or 1000Base-X
- RJ45 for 10/100/1000Base-T
- UART console (USB)
- 6V-30V DC (Power supply included)
- 2x PMOD connectors

7-Series Kit:

1588-aware HSR/PRP/Ethernet Switch Module

Embedded Software



SoC-e Portable Tools

In order to simplify the integration and the use of IP technology, SoC-e has developed a portfolio of portable software solutions. This portability allows implementations on reconfigurable SoC platforms, embedded CPUs or on PC systems. The following list summarizes the software modules that integrate the SoC-e Portable Tools:

- Switch Management API
- SNMP Switch Management module
- WEB Switch Management module
- Network supervision module
- PTP software stack
- RSTP Linux stack

RSTP Posix-compliant Software Stack

SoC-e RSTPdstack is a portable C language, POSIX compatible, which implements RSTP processing according to the IEEE802.1D-2004 standard. The integration on Unix or VxWorks OS systems is straightforward. It can be used in combination with SoC-e MES IP or with other switches able to handle BDPU frames.

Key features:

- It implements IEEE 802.1D standard and processes all RSTP related events such as:
- Reception of a BPDU
- Identification of Physical Link status change
- Management of timeout 1 second
- Changes in the bridge parameters

As result of any of these events, the RSTP priority vectors and timing vectors are recalculated and the following actions are performed:

- Transmission of BPDUs
- Switch's MAC table clearing
- Change in switch's ports status

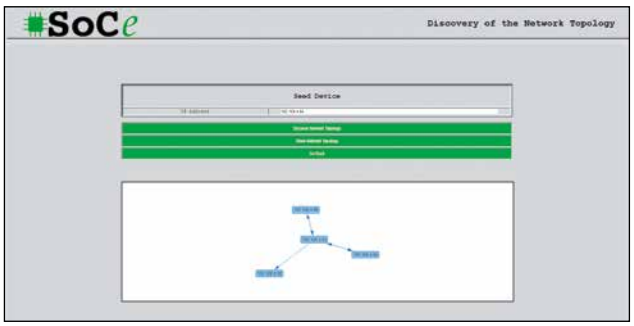
Embedded Software

Layer-3 Routing Package

The complexity of current networks demands going beyond Layer-2 switching. SoC-e Layer-3 Routing Package (L3RP) is a supported software package for Linux that can take benefit for SoC-e networking IP cores or run in full software Linux based embedded system. L3RP is focused on implementing the most usual functions for a low-latency Layer-3 switch.

Key features:

- Static Routing
- Dynamic Routing (BGP, OSPF)
- Multicast IP routing
- IGMP Snooping
- IPv4 & IPv6
- DHCP Server & Client
- NAT



Cybersecurity Embedded Package

SoC-e simplifies the integration and maintenance of the widely used mechanism for security on Linux Embedded systems focused on networking.

SoC-e Cybersecurity Embedded Package (CEP) includes among other services: TPM-aware X.509 Certificates management, Firewall, NAT, VPN, and SIEM agent integration.

CEP is a valuable add-on for solutions based on reconfigurable SoPCs that integrate SoC-e networking, synchronization or security IPs and need to be completed with a supported security package.

Key features:

- TPM integrated circuit root-of-trust management
- Network security services: Firewall, NAT, VPN, etc.
- Security events collection, normalization and correlation
- Intrusion detection
- Network use behavioral monitoring

Embedded Software

IEC 62351-9 Stack: Key Management for Substation Automation Systems

The early implementations of secure networks in unattended critical systems have faced a common challenge: how to manage and distribute properly the security keys. These OT networks are composed of heterogeneous embedded devices that should be a potential destination of security keys if secure control messages need to be used by them.

The electric sector demands an adequate Key Management scheme that addresses the specific requirements pof this industry. Recently, IEC has released the IEC 62351-9 standard. It specifies how the security keys and certifies need to be managed and distributed.

SoC-e has developed a software package that comprises all the modules required to implement IEC 62351-9 standard in an Embedded System. This package supports SoC-e Substation Automation Systems Crypto-core IP providing all the security keys required for secure critical control traffic.

Key features:

- TPM security IC root-of-trust support
- Asymmetric Key Manager (AKM) module to manage:
  - Public Key Infrastructure (PKI)
  - Inventory and equipment enrolment
  - Certificates and signatures
- Symmetric Key Manager (SKM) module to manage:
  - Key interchange with Key Distribution Center Server (KDC)
  - IEC GDOI Server
- Autonomous key management for IEC 62351-6 SAScrypt IP to secure GOOSE and SMV frames

Tailored Solutions

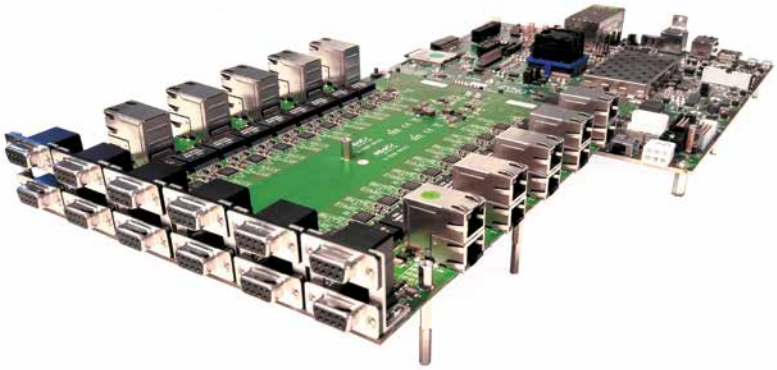
The SoC-e Team accumulates thousands of man-hours applied to FPGA and complex embedded system designs. The specialization on time-aware Networking solutions implemented on latest generation FPGAs has positioned SoC-e as a trustable partner for turn-key projects focused on Industry and Aerospace sectors. The scope of these projects can vary since IP integration till full board and embedded system design. The three following examples highlight these capabilities.

VPX Sofware Defined Radio Platform

Complete SDR conduction-cool and laboratory VPX system design and production.

PCIe Systems for HSR/ PRP/TSN

Smart PCIe subsystems for specialized networking configurations for critical-mission systems and OT/IT integration.



Multi-Gigabit/CAN/Lin Ethernet FMC Card

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