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Supporting Accurate Synchronization for Telecom Profiles: 5G

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ABSTRACT 5G needs to manage multiple timing sources across the network. Synchronizations below 1us are required, and the dependence on GPS should be minimized.

KEYWORDS
5G
RAN
Ethernet
IEEE 1588
FPGA
G.8275.2/.1

INTRODUCTION

Time Division Duplex (TDD) spectrum requires a tight time and phase synchronization to avoid interference between the uplink and downlink. Additionally, many other features of these new generation RAN Networks require synchronization accuracy in the range on 1us and below. As an example, the Coordinated multipoint (CoMP) transmission/reception technology needs a relative time sync between neighboring radios lower than 1us or the NR-TDD Beam-forming needs that the synchronization across the whole network were maintained approximately in 1,5us.

In order to support this global accurate synchronization, the recommendation from the telecom operators [1] is evolving to networking infrastructures that combine GPS sources for timing and Full Timing Support (FTS). FTS is a profile on Precise Time Protocol- IEEE 1588v2 (PTP)- IEEE 1588v2 [2]. Figure 1 summarizes the timing requirements for the 5G transportation network.

PTP offers an accurate and redundant network distribution. It uses the Layer-2 and Layer-3 Network infrastructure used for the data. However, all the switching and routing equipment should be 1588-aware devices. This is, they shall support Transparent or Boundary Clocks. Specifically, the Telecom Boundary and Slave Clocks as defined in the Assisted Partial Timing Support (G.8275.2) [3] and Full Timing Support (G.8275.1) PTP profiles.

In **System-on-Chip** *engineering* we provide technology to embed PTP and 1588-aware Ethernet switching capabilities on any networking equipment. As an example, the following use-case will present how to implement a Telecom Slave-Clock using **SoC***e* PreciseTimeBasic (PTB) IP core [5].

IMPLEMENTING TELECOM CLOCKS USING PTB IP CORE

PreciseTimeBasic (PTB) is a IEEE1588-2008 v2 compliant clock synchronization IP core for Xilinx FPGAs. It is capable of accurately time stamp Layer-2 and Layer-3 IEEE 1588 telegrams and provide a compatible timer. All these processes are carried out by hardware modules.

This product supports the following PTP-IEEE 1588v2 profiles. Industrial Profiles: Default, Power, Power-Utility IEC 61850-9-3, IEEE 802.1AS. Automotive profile: IEEE 802.1AS general PTP (gPTP) profile. Enterprise profile/5G/Telecom profiles: G.8265.1, G.8275.1, and G.8275.2.

For 1G networks, the IP is located between the internal Ethernet

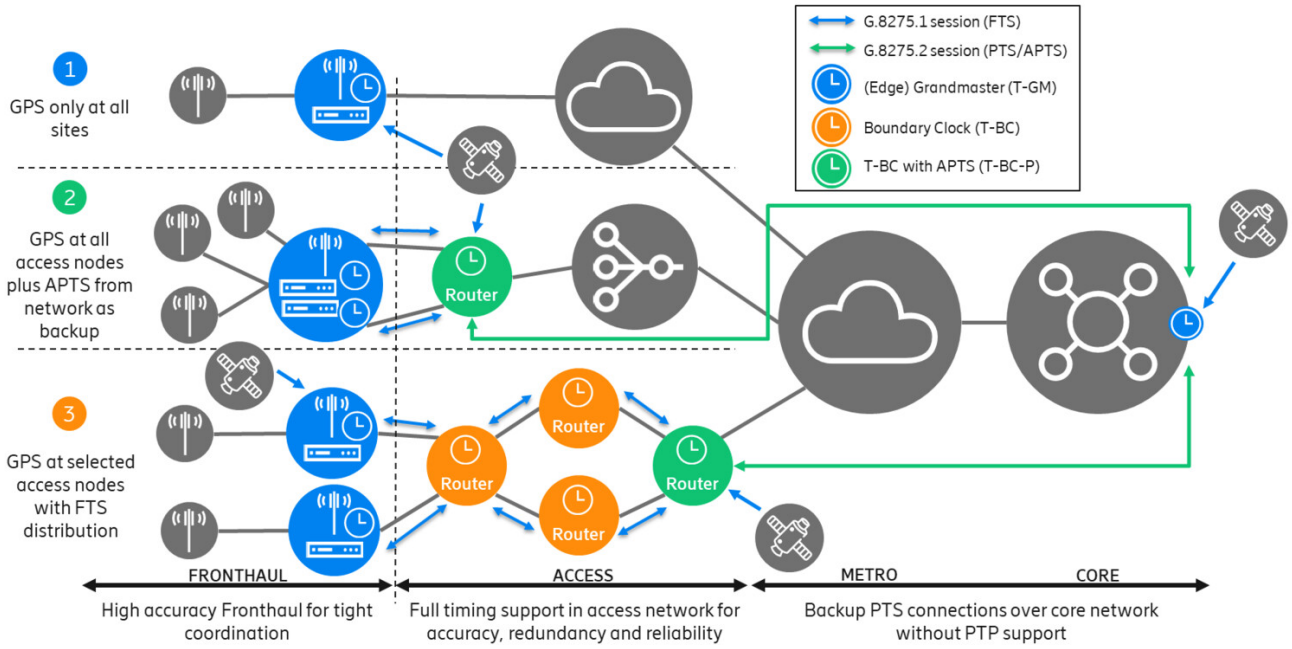

Figure 1 Timing requirements for the 5G transportation network [1].

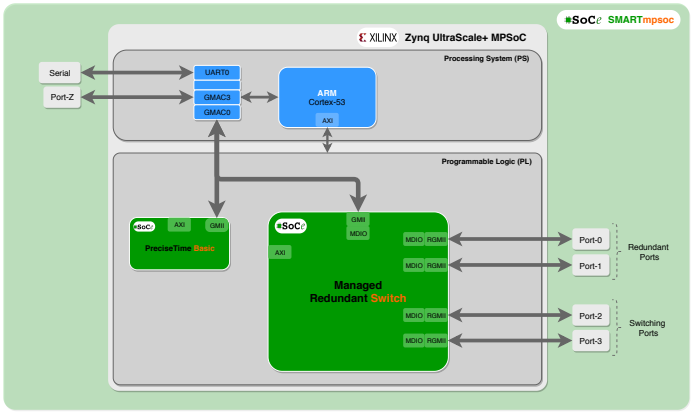

Figure 2 PTB IP integrated in a SoC to support IEEE 1588v2 Ordinary Clock features

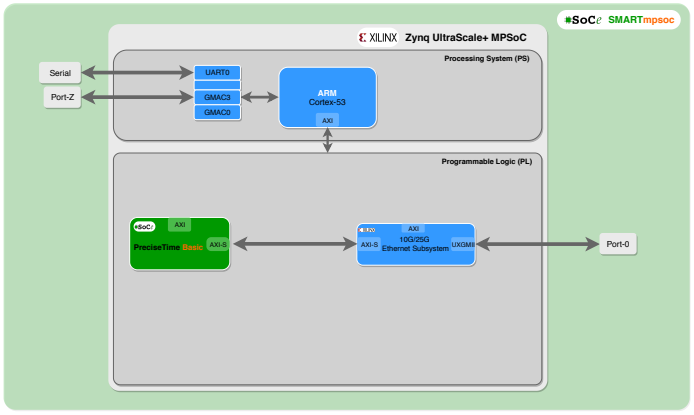

Figure 3 PTB IP connected to a 10G/25G Ethernet MAC subsystem for Ordinary Clock operation

MAC or the embedded switch and the external PHY. PTB parses all the Ethernet frames, inspecting which ones are IEEE 1588. This IP provides a PTP Hardware Clock (PHC) compatible device for the software processing. This software is in charge of maintaining the PTP timer. This infrastructure is represented in Figure 2. In this case, the connectivity with the Ethernet network is done through **SoC***e* Managed Redundant Switch (MRS) IP core that supports standard Ethernet and zero-delay recovery time Ethernet (HSR/PRP) [4].

For 10G and 25G systems, the IP is responsible for the same tasks as described previously. However, it is connected directly with the 10G/25G capable MAC or switch through a dedicated AXI-steam interface. This infrastructure is represented in Figure 3 to support Master and Slave Clock operation. Figure 4 proposes a set-up for a Boundary Clock implementation based on two Xilinx 10G/25G Ethernet subsystems combined with **SoC***e* PTP IPs.

The behavioral of these solutions can be evaluated using **SoC***e* bricks based on Xilinx Zynq-7000 SoC or Ultrascale+ MPSoC. Figure 5 shows the SMARTmpsoc brick.

In order to receive more information about SoC-e solutions for networking, synchronization and wire-speed cybersecurity, please contact SoC-e team at info@soc-e.com.

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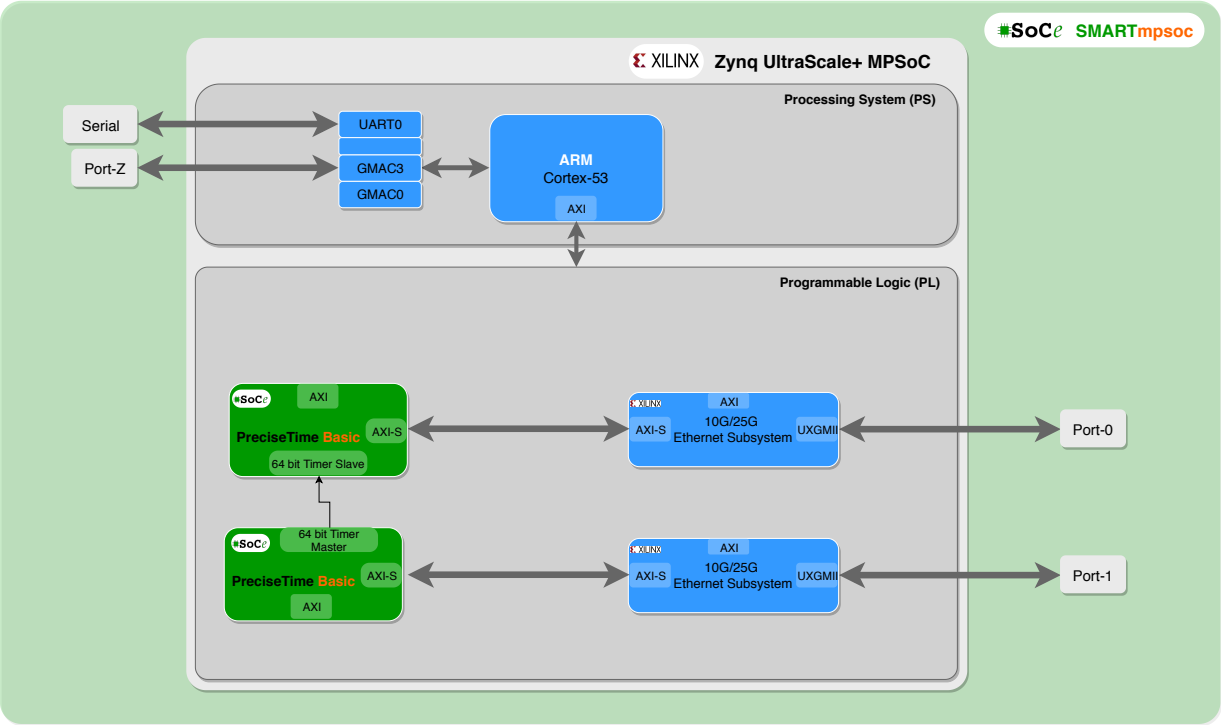

Figure 4 PTB IP connected to two 10G/25G Ethernet MAC subsystems for Boundary Clock operation

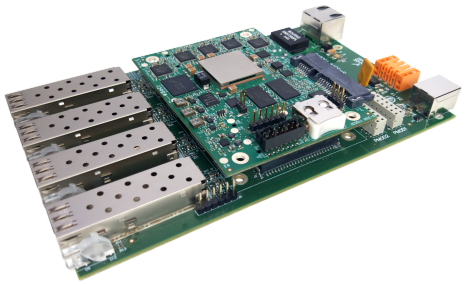

Figure 5 SoCe SMARTmpsoc Brick development platform.

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