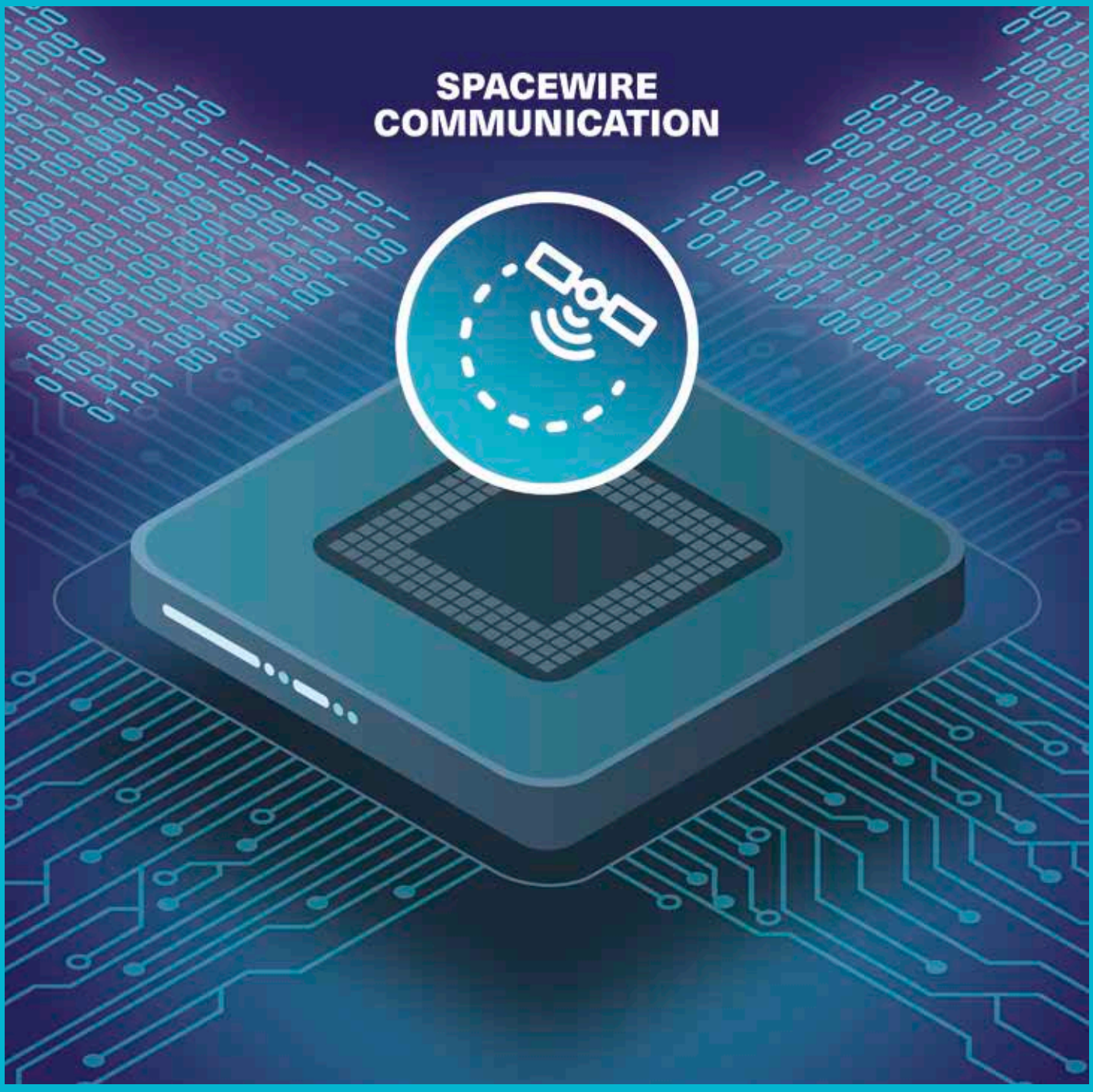
SocTek® IP Cores



SpaceWire Node IP core

SPWN

Overview

The SpaceWire IP Core implements a complete, reliable and fast SpaceWire encoder-decoder which has been designed according to ECSS-E-ST-50-12C.

SpaceWire protocol is a standard for high-speed links and networks for use in on-board spacecraft, easing the interconnection of sensors, mass-memories, processing units and downlink telemetry sub-systems. It is a full-duplex, bidirectional, serial, point-to-point data link. It encodes data using two differential pairs in each direction. That is a total of eight signal wires, four in each direction.

The SpaceWire RDDP (reliable data delivery protocol) is applicable to many aerospace microelectronics devices like spacecraft systems, nano satellites (i.e. CubeSat), space cameras, OBC (On Board Computer) and embedded microcontrollers.

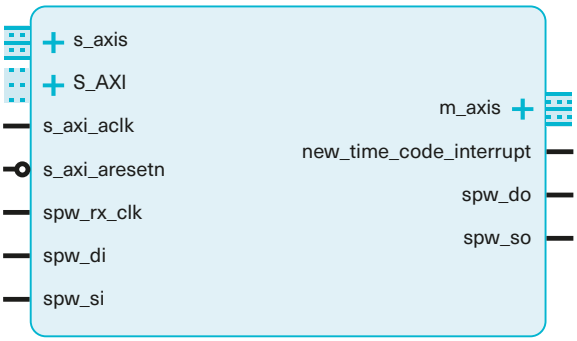
This IP core can operate up to the packet level in point-to-point links, without requiring any destination address.

SpaceWire IP Core has been designed all-in RTL (VHDL), without the requiring an external microprocessor or software for encoding / decoding in order to reduce the required gate & memory.

Key Features

- SpaceWire Encoder-Decoder: it implements a complete, reliable and fast SpaceWire encoder-decoder designed according to ECSS-E-ST-50-12C.
- IP “Builder”: dozens of user-configurable parameters allow obtaining the exact configuration required by the customer, ensuring efficient use of the available programmable logic resources.
- Fast & Smooth Integration: GUI available for FPGA vendor tools (i.e., AMD Vivado™ Design Suite). Linux drivers for AMD / Xilinx Zynq®-7000 & Zynq®UltraScale+ MPSoC included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Standard Interfaces

- Designed to conform to ECSS-E-ST-50-12C
- Two possible implementations for receiver and transmitter that provide high speed operation up-to 200 Mbps
- Separate clock domains
- Simple, byte-wide FIFO interface to RX and TX buffers
- Configurable Tx FIFO depth: From 64 bytes to 16384 bytes
- Configurable Rx FIFO depth: From 64 bytes to 16384 bytes
- Time-codes supported

Communication Interfaces

- AXI-Stream data interface with a data width of 8 bits @ 125 MHz

Management & Monitoring

- AXI-4 Lite management interface to access control and statistics registers

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Software components: Drivers, configuration API & SW stacks
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Ordering Code

Ordering code
S-3132 (SPWN IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

SPWN

SpaceWire Node IP core

SOC-E®

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