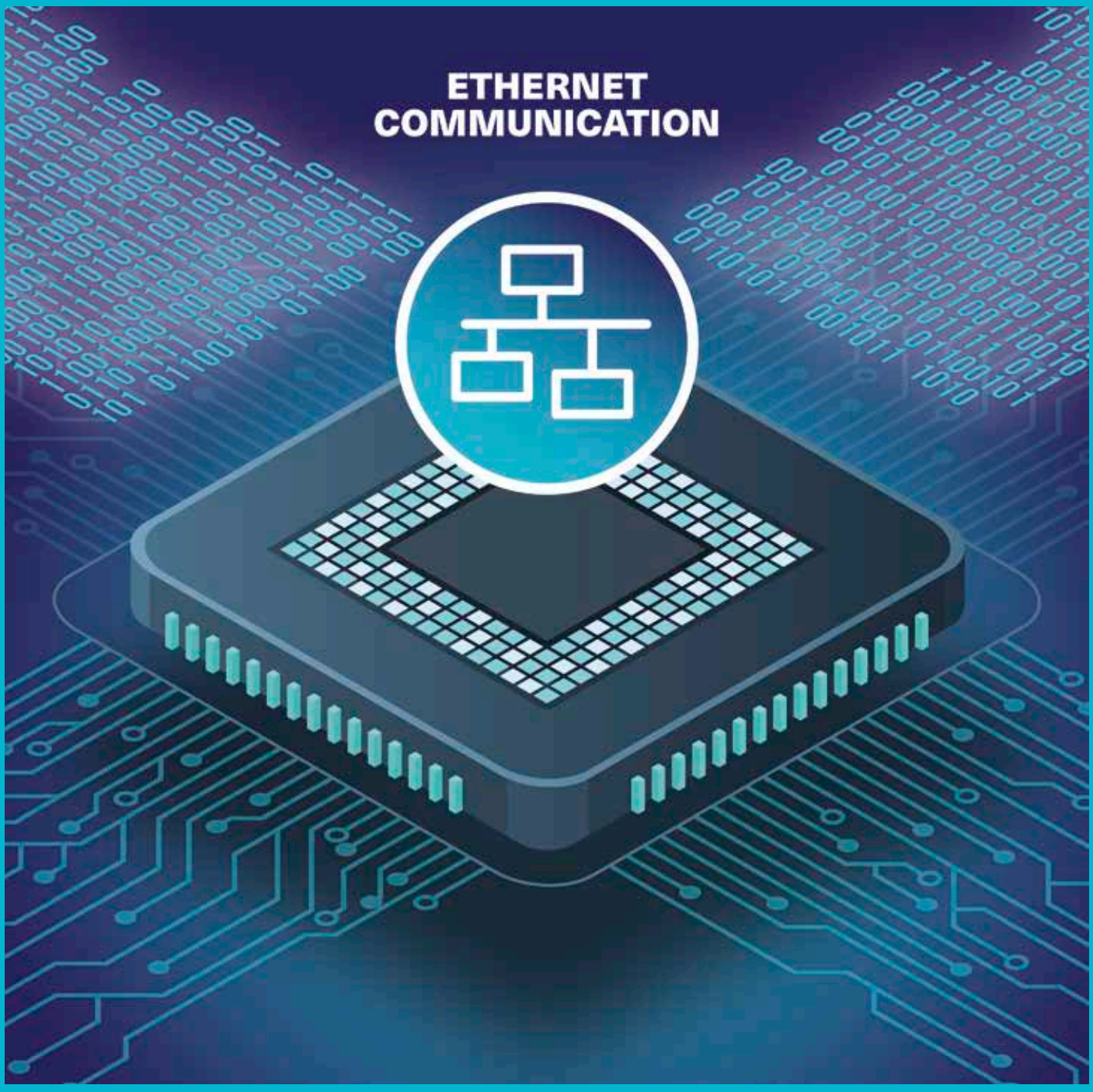
SocTek® IP Cores



100M/1G/10G
TSN Endpoint IP Core

ETSN

Overview

ETSN provides Time-Sensitive Networking (TSN) capabilities to devices that operate as end systems in the network. End systems typically behaving as the source (talker) and/or sink (listener) of the data that is exchanged within the network.

With a rich set of layer-2 configurable features, both at synthesis time & during runtime, ETSN allows building advanced end systems with TSN capabilities. ETSN switch has been designed to address the maximum throughput using optimized resources.

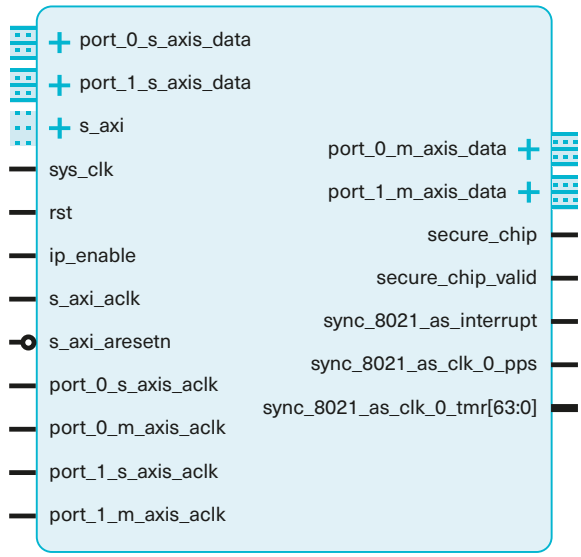
The internal micro-architecture includes disruptive enhancements in order to ensure a reliable operation of the endpoint even in critical use-cases.

All these characteristics enable a wide number of applications/sectors where the use of ETSN IP Core is key. Automotive, Marine, Aerospace, Defence or Electric are examples of markets where our customers are already applying this technology.

Key Features

- Time-Sensitive Networking (TSN) support: aligned with the different TSN profiles, such as Aerospace (P802.1DP), Automotive (P802.1DG) or Industrial Automation (IEC/IEEE 60802).
- IP “builder”: hundreds of user-configurable parameters allow obtaining the exact configuration required by the customer, ensuring efficient use of the available programmable logic resources.
- Fast & smooth integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite). Drivers & software components included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™ QSGMII IP core respectively
- Configurable AXI-Stream interfaces to support several data rates:
  - 10/100/1000 Mbps AXI-S interface with a data width of 8 bits @ 125 MHz
  - 10/100/1000/2500/5000/10000 Mbps AXI-S interface with a data width of 32 bits @ 312.5 MHz
  - 10/100/1000/2500/5000/10000 Mbps AXI-S interface with a data width of 64 bits @ 156.25 MHz
- Compatible with USXGMII (Universal Serial 10GE Media Independent Interface) or 10GBASE-R PHY interfaces throughout an internal AXI-S based connection to AMD LogiCORE™ USXGMII IP core and LogiCORE™ 10G/25G Ethernet Subsystem IP core respectively

Time-Sensitive Networking (TSN)

- TSN features can be enabled/ disabled independently
- IEEE 802.1AS - Timing and Synchronization (gPTP)
- IEEE 802.1Qav - Credit Based Shaper (CBS)
- IEEE 802.1Qbv - Time Aware Shaper (TAS)
- IEEE 802.1Qci - Per-Stream Filtering and Policing (PSFP)
- IEEE 802.1CB - Frame Replication and Elimination for Reliability (FRER)
- IEEE 802.1Qcc - Stream Reservation Protocol (SRP) Enhancements and Performance Improvements

Time Synchronization

- Time synchronization according to IEEE 802.1AS-2020 (gPTP) and IEEE1588 (PTP)
  - Up to four IEEE802.1AS time domains
- Legacy PTP: IEEE1588 Transparent Clock (TC) functionality (End-to-End or Peer-to-peer) at layer-2 and layer-3 (IPv4)
- Legacy PTP: IEEE 1588 Boundary Clock (BC) at layer-2 and layer-3 (IPv4)

Traffic Management

- Resource sharing algorithm (executed at synthesis time) to define the optimal internal architecture to reduce resource usage without performance compromises
- Shared dynamic and static filtering database. Implements hardware MAC address learning/ageing and look-up for up to 9K absolute MAC addresses (synthesis scalable) at wire speed
- Independent VLAN Learning support for MAC address learning
- Searchable MAC addresses (and associated information) contained in the filtering database
- Static multicast frame filtering
- IGMP v1/v2 snooping1 (IPv4) support for multicast frame filtering
- Standard frame size support (1518) or Jumbo frames up to 9 kByte (depends on memory availability)

Quality of Service

- Up to 8 priority queues per port (synthesis option)
  - Priority classification based on PCP bits (802.1p), DSCP TOS bits of the IP packets (IPv4 TOS / IPv6 COS) and EtherType
  - Programmable remapping from PCP or DSCP fields to internal priority queues on a per-port basis
  - Programmable priority regeneration on a per-port basis
  - Egress traffic prioritization based on strict priority or Weighted Round Robin (WRR) scheduling algorithm
- IEEE 802.1Q tag-based and port-based VLANs. VLAN manipulation functions on reception (VLAN insertion) and transmission (VLAN removal/overwrite)
- MAC level ingress frame filtering based of destination MAC address and/or EtherType on per port basis
- Token bucket based ingress throughput rate limiting on per port basis
- MAC level ingress frame rate limiting on per port basis
- Credit Based Shaper (CBS) egress throughput rate Limiting on per port basis
- Egress frame rate limiting on per port basis
- Broadcast/Multicast storm protection

Network Management & Monitoring

- IEEE 802.1D Spanning-Tree Protocol (STP) to prevent loops from being formed when switches or bridges are interconnected via multiple paths
- IEEE 802.1w Rapid Spanning Tree Protocol (RSTP) provides rapid convergence of spanning tree
- IEEE 802.1s Multiple Spanning Tree Protocol (MSTP) provides link availability in multiple VLAN environments by allowing multiple spanning trees
- Port mirroring capabilities. Ingress and egress mirroring functions to allow copying of frames to a mirror port. Option for mirroring only filtered frames that match a specific data pattern
- Per port MAC and switch statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)

Others

- Distributed Switch Architecture (DSA) frame tagging to merge application specific messages to management port and to distribute application specific messages to a specific port
- Exclusive forwarding of known protocol specific frames or custom frames to/from management port

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity/Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted/Source RTL code
- Software components: drivers, configuration API & SW stacks
- Documentation (IP Core and software components)
- (Optional) Networking Testbench Suite (NTS)
- (Optional) AMD Vivado™ design suite example design

Related Products

- Networking Testbench Suite (NTS)
- 1G TSN Ethernet Switch (MTSN IP Core)
- 10G TSN Ethernet Switch (TGES IP Core)

Ordering Code

Ordering code
S-3139 (ETSN IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

ETSN

100M/1G/10G
TSN Endpoint IP Core

SOC-E®

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