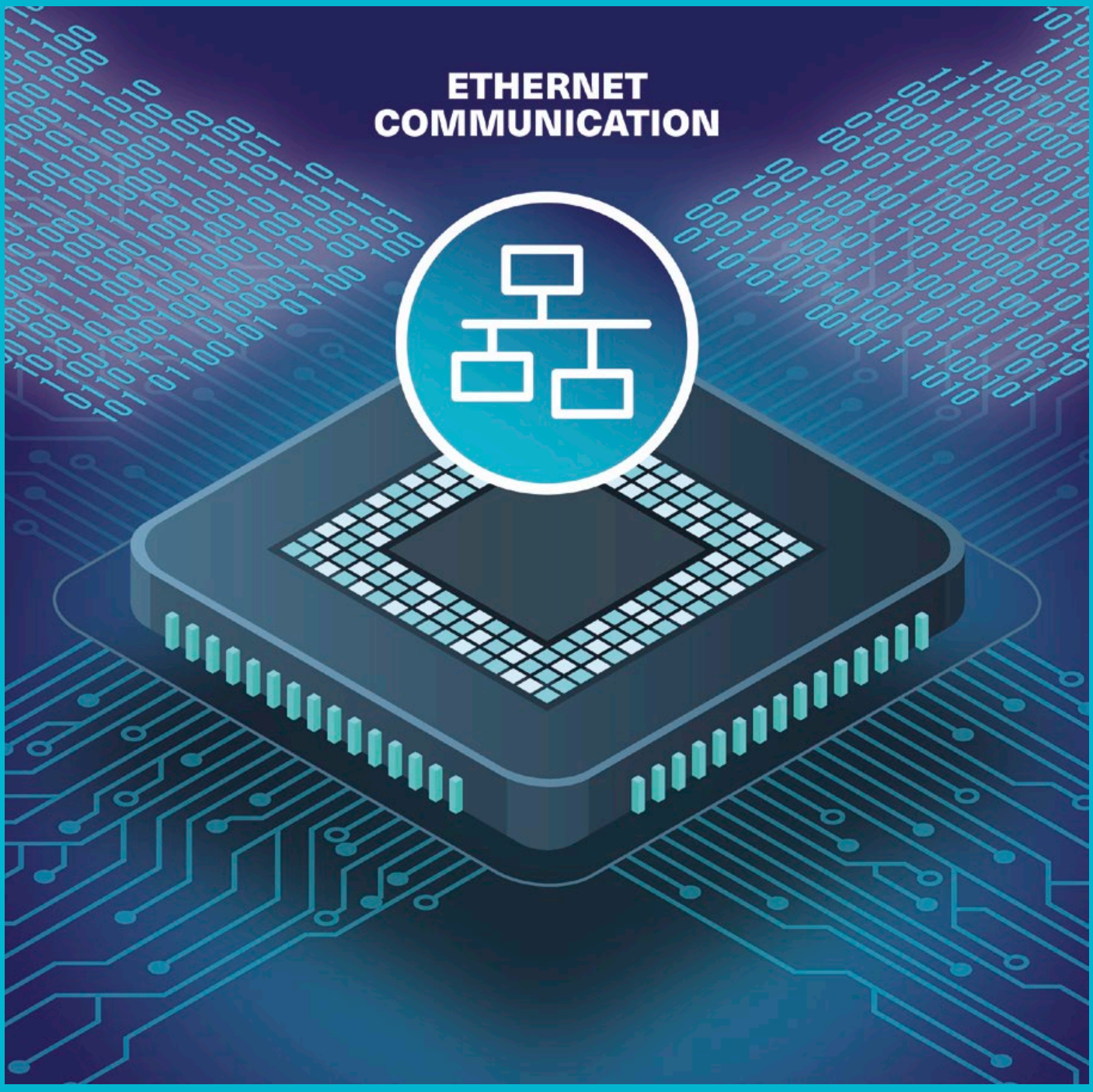
SocTek® IP Cores



10M/100M/1G
HSR-PRP Switch IP Core

HPS

Overview

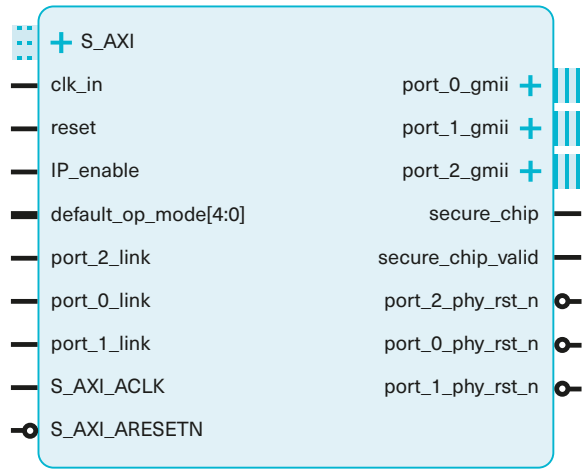
HPS implements the High-availability Seamless Redundancy and Parallel Redundancy Protocol (HSR and PRP, IEC 62439-3 Clause 5 and 4 respectively) Edition 4.0 protocols for Reliable Ethernet communications providing zero recovery time.

It is a full hardware solution that can be implemented in different FPGA families, including low-cost versions. It is a flexible solution for the Electric sector equipment that require to be connected to HSR rings, PRP Lans or to operate as network bridges.

Key Features

- Zero recovery time redundancy protocol support: the IP core implements HSR and PRP redundancy protocols (IEC 62439-3) providing seamless Ethernet redundancy.
- Lowest latency in HSR: thanks to the implementation of cut-through between ring ports.
- High-performance: Up-to 1G interfaces.
- Fast & smooth Integration: Fast & smooth Integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite) included as part of the product deliverable.
- Evaluation version available: Encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, RMII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™ QSGMII IP core respectively
- 10/100/1000 Mbps AXI-Stream interface with a data width of 8 bits @ 125 MHz

Redundancy

- High-availability Seamless Redundancy (HSR). It can operate in any of the following modes, which are changeable at runtime:
  - Mode H (mandatory, default mode): HSR-tagged forwarding
  - Mode M (optional): mixed forwarding HSR-tagged and non HSR-tagged
  - Mode N (optional): no forwarding
  - Mode T (optional): transparent forwarding
  - Mode U (optional): unicast forwarding
  - Mode R (optional): for RedBoxes to be connected to an RSTP bridge
- Parallel Redundancy Protocol (PRP). It can operate in any of the following modes, which are changeable at runtime:
  - Duplicate Discard (default mode)
  - Duplicate Accept (testing only)
- In HSR mode, the RedBox can work on one of the following three modes:
  - HSR-SAN: the traffic on the interlink is not HSR, not PRP
  - HSR-PRP: the traffic on the interlink is PRP-tagged
  - HSR-HSR: the traffic on the interlink is HSR-tagged
- Configurable size redundancy proxy node table to keep information about all nodes that are attached to the interlink port
- Configurable size redundancy duplicate discard table used to discard duplicate frames received from redundant ports

Time Synchronization

- IEEE1588 (PTPv2): IEEE1588 Stateless Transparent Clock (SLTC) functionality at layer-2 and peer-to-peer (P2P)
- IEEE1588 Hybrid Clock (HC) slave-only support:
  - IEEE 1588-2008 (PTPv2) slave-only compliant clock synchronization
  - One Pulse-Per-Second (PPS) output available
  - Event timestamping supported (up-to 4 different events simultaneously)
  - Alarm detection supported (up-to 4 different alarms simultaneously)
- IRIG-B Master support:
  - IRIG 200-04 compliant time synchronization master
  - Support for DCLS modulation
  - Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
  - IEEE1344 extension support
  - Output type (IRIG-B time code) configurable both before implementation and on the fly
  - Implements a generic DAC controller compatible with SPI, QSPI and MICROWIRE protocols

Traffic Management

- Cut-through forwarding between redundant ring ports for a very low forwarding latency independent from frame size
- MAC level ingress frame filtering based of destination MAC address and/or EtherType on per port basis
- Custom destination MAC filtering and forwarding (up to 16 MAC addresses can be filtered)
- Custom source MAC filtering and forwarding (up to 10 MAC addresses can be filtered)
- Standard frame size support (1518) or Jumbo frames up to 9 kByte (depends on memory availability)

Quality of Service

- QoS support with up to 8 priority queues per port (synthesis option):
  - Priority classification based on ingress port, PCP bits (802.1p), DSCP TOS bits of the IP packets (IPv4 TOS/IPv6 COS) and EtherType
  - Programmable remapping from PCP or DSCP fields to internal priority queues on a per-port basis
- Traffic prioritization based on strict priority scheduling algorithm
- MAC level ingress frame rate limiting on per port basis

Network Management & Monitoring

- Per port MAC and switch statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)
- I2C master interface for external device configuration (i.e. an EEPROM memory with non-volatile configuration)

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity/Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted/Source RTL code
- Software components: Drivers, configuration API & SW stacks
- Documentation (IP Core and software components)
- (Optional) Networking Testbench Suite (NTS)
- (Optional) AMD Vivado™ design suite example design

Evaluation & Design-in Kit

Description

The SMARTmpsoc and SMARTzynq Brick provide an out-of-the-box set-up that allows plug & play evaluation of HSR and PRP protocols. The evaluation board is provided with a preloaded firmware that includes an instance of SOC-E IP Core(s) plus additional software components that are executed in the processing system (CPU) of the platform. Linux OS is loaded in the evaluation firmware.

This hardware can also be used later as a development platform, what allows to shorten the development phase.

- SMARTmpsoc Brick consists of the following package:
  - SMARTmpsoc module (1x)
  - Carrier board (1x)
  - Reference firmware (predefined image) preloaded into non-volatile eMMC storage (1x)
  - Power supply (1x)
  - Fibre/Copper SFP modules (optional, purchased separately)

- SMARTzynq Brick consists of the following package:
  - SMARTzynq module (1x)
  - Carrier board (1x)
  - Reference firmware (predefined image) preloaded into non-volatile microSD card storage (1x)
  - Power supply (1x)
  - Fibre/Copper SFP modules (optional, purchased separately)

Related Products

- Networking Testbench Suite (NTS)
- 1G Managed Redundant Switch (MRS IP Core)

Ordering Code

Ordering code
S-3111 (HPS IP Core)
EVB07.27 (SMARTmpsoc Brick)
EVB04.28 (SMARTzynq Brick)

To know more about other available references, please contact your sales representative.

SocTek®

By

HPS

10M/100M/1G
HSR-PRP Switch IP Core

SOC-E®

www.soc-e.com
info@soc-e.com

Calle Islas Canarias 19, piso -1
48015 Bilbao (Spain)