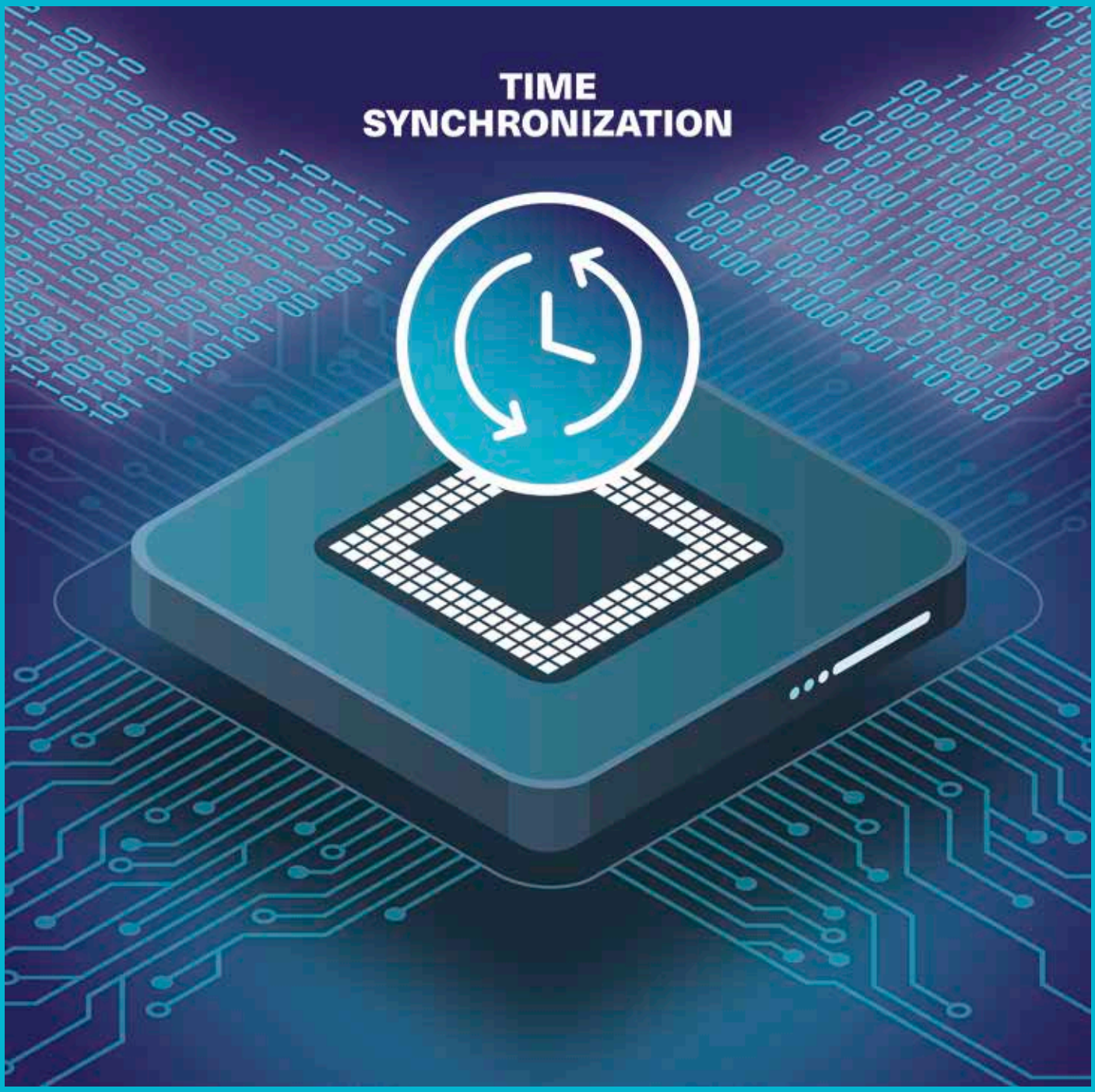
SocTek® IP Cores



IRIGtimeM IP Core

ITM

Overview

ITM is an IRIG 200-04 compliant time synchronization master / time transmitter for FPGA. This IRIG-B master / time transmitter IP has been designed to support multiple IRIG-B coded expressions as well as DCLS modulation in order to provide maximum flexibility.

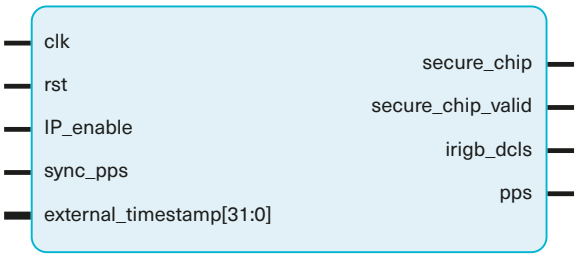
ITM can be configured to support the most extended IRIG-B time codes to provide higher compatibility with the majority of IRIG-B slaves / time receivers in the market. This configuration can be done before implementing the IP by selecting the desired modulation type, carrier frequency, coded expression and other parameters in the FPGA design tool as well as during runtime using register based configuration.

It has been designed as a hardware-only (VHDL) IP Core. No microprocessor or software is required in order to reduce integration complexity.

Key Features

- Multiple time code support: including year information, control functions and straight binary seconds.
- PPS and 10MHz inputs available: for synchronizing to high precision external clocks.
- IEEE1344 extension supported.
- Fast & smooth Integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite).
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Time Synchronization

- IRIG 200-04 compliant time synchronization master
- Support for DCLS modulation
- Output type (IRIG-B time code) configurable both before implementation and on the fly
- High accuracy 64-bit internal timer architecture that allows IRIG-B slaves to synchronize to the master in the range of nanoseconds
- PPS and 10MHz synchronization inputs available

Management & Monitoring

- AXI4-Lite or UART management interfaces to access control registers (selectable at synthesis time)

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Related Products

- Slave IRIG-B (IRIGtimeS IP Core)

Ordering Code

Ordering code
S-3115 (IRIGtimeM IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

ITM

IRIGtimeM IP Core

SOC-E®

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