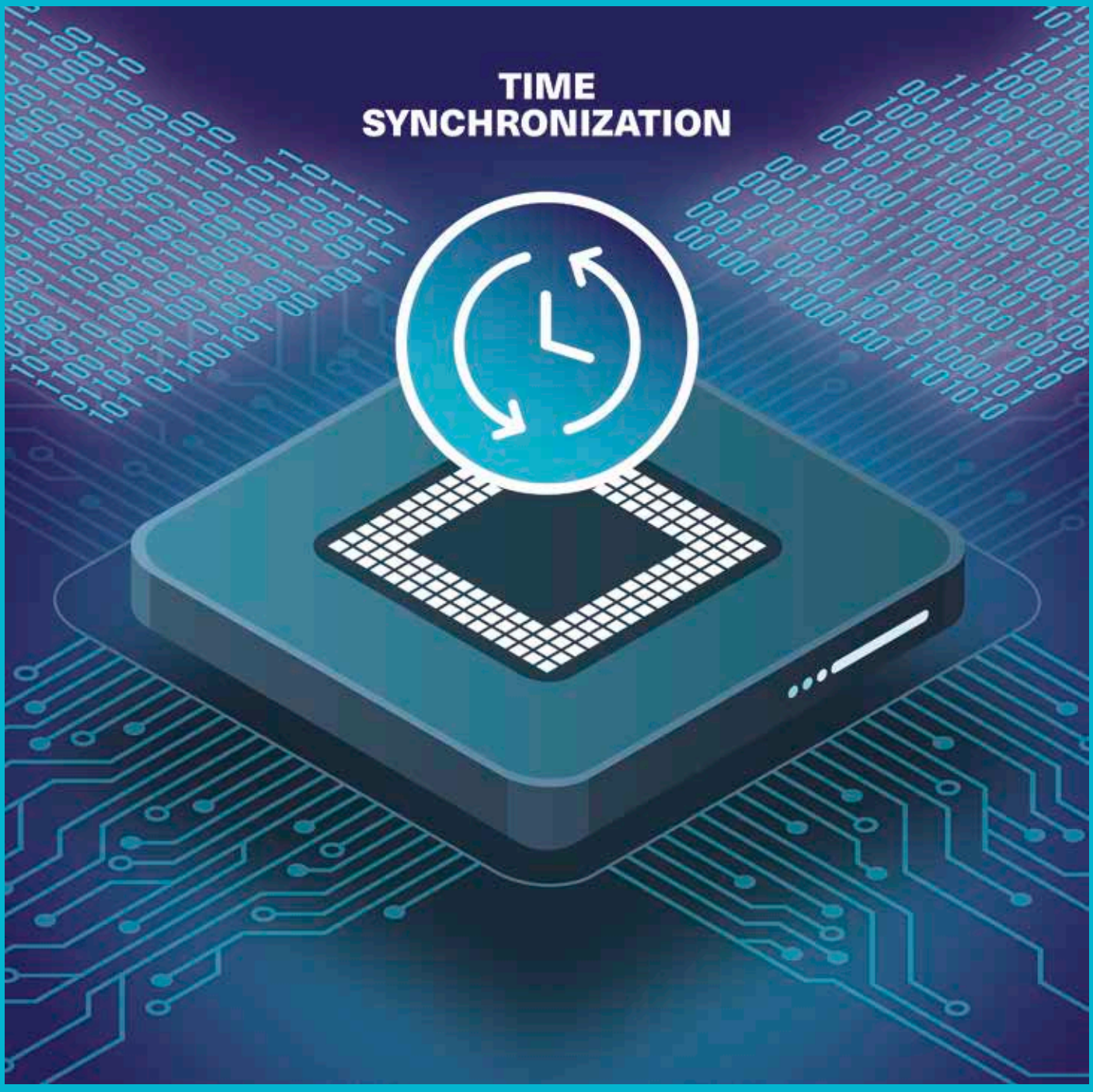
SocTek® IP Cores



MULTIsync IP Core

MSYNC

Overview

MULTIsync is a multi-protocol time synchronization IP Core with redundancy capabilities that provides sub-microsecond time synchronization, ensuring maximum flexibility for every scenario.

On one hand, MULTIsync is able to provide time synchronization in the range of nanosecond accuracy over an Ethernet network using IEEE 1588 (PTP) time synchronization protocol.

On the other hand, this solution implements an IRIG 200-04 compliant IRIG-B master / time transmitter & slave / time receiver module (a simple serial time synchronization protocol that provides sub-microsecond accuracy) in order to provide time synchronization in less complex scenarios and ensure compatibility with legacy equipment.

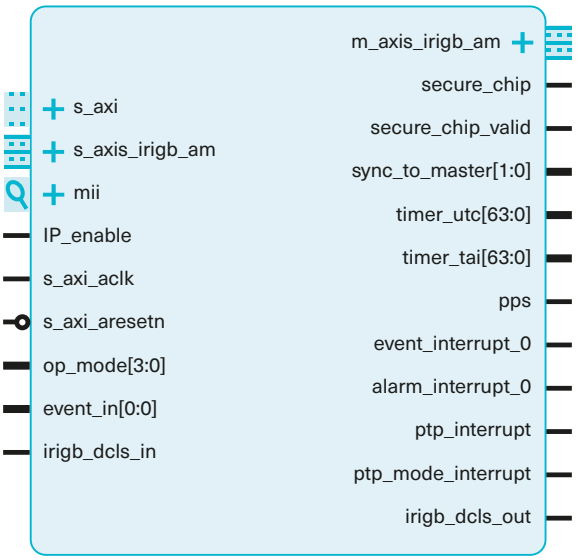
This solution is composed by three main components: An IP Core for FPGA that implements the timestamping unit (TSU); a PTP stack for Linux operating system (running on the in-built SoPC processor) and a driver (provided as a patch for Linux kernel).

MULTIsync IP Core is specifically designed for AMD/Xilinx SoPC platforms, specifically Zynq®-7000 & Zynq®UltraScale+ MPSoC families.

Key Features

- Time synchronization redundancy: making possible to connect the IP to a PTP network and IRIG-B master / time transmitter at the same time. The user can select which is the time source used between the three available (PTP, IRIG-B, free running timer).
- Time bridge / gateway: operate as a PTP to IRIG-B or IRIG-B to PTP bridge while the IP is synchronized with the selected master.
- Fast & smooth integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite). Drivers & software components included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™QSGMII IP core respectively
- Configurable AXI-Stream interfaces to support several data rates
  - 1000/10000/25000 Mbps AXI-S interface with a data width of 64 bits @ 156.25 MHz

Time Synchronization

- Multi-protocol & redundant time synchronization
- IEEE1588 (PTP) and IRIG-B time synchronization protocol supported simultaneously
- 12 different operation modes
- 3 independent 64-bit adjustable timers associated to each slave:
  - PTP slave / time receiver timer
  - IRIG-B slave / time receiver timer
  - Free running timer (managed by the user)
- One Pulse Per Second (PPS) output available
- Layer-2 (PTP over ethernet) and Layer-3 (PTP over UDP) supported
- Event timestamping supported (up to 4 different events simultaneously)
- Alarm detection supported (up to 4 different alarms simultaneously)

IRIG-B Slave

- IRIG 200-04 compliant time synchronization slave / time receiver
- Support for DCLS modulation
- Input type (IRIG-B time code) configurable both before implementation and on the fly
- Sub-microsecond synchronization with the IRIG-B master
- 64-bit internal timer synchronized in time and frequency with the IRIG-B master:
  - 32-bit for timestamp in seconds and 32-bit for nanoseconds

IRIG-B Master

- IRIG 200-04 compliant time synchronization master / time transmitter
- Support for DCLS modulation
- Output type (IRIG-B time code) configurable both before implementation and on the fly
- High accuracy 64-bit internal timer architecture that allows IRIG-B slaves to synchronize to the master in the range of nanoseconds
- PPS and 10MHz synchronization inputs available

Free Running Timer

- Fully managed by the user (time and frequency adjustment)
- Dedicated 32 bit seconds / 32 bit nanoseconds timer
- 32 bit sub-nanosecond frequency adjust

Network Management & Monitoring

- Per port MAC statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Software components: drivers, configuration API & SW stacks
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Related Products

- PreciseTimeBasic (PTB IP Core)
- 1588Tiny IP Core
- Master IRIG-B (IRIGtimeM IP Core)
- Slave IRIG-B (IRIGtimeS IP Core)

Ordering Code

Ordering code
S-3128 (MULTIsync IP Core)

To know more about other available reference[illegible]ase contact your sales representative.

SocTek®

By

MSYNC

MULTIsync IP Core

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