Nanosecond Accuracy using SoC Platforms

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***Abstract*—In this work, the implementation of IEEE 1588 functionalities on new Xilinx Zynq-7000 All Programmable SoC device is explored. An experimental set-up based on two Zynq commercial low-cost boards, with different PTP master and slave implementations has been analysed, taking benefit from the flexibility of the SoC all programmable devices. The explored features go from the only-software versions aided by the IEEE 1588-aware GMACs embedded in the processor sections to the high-accuracy solutions that combine the IEEE1588 hardware stuff of these modules with custom PTP IP cores in the FPGA sections of the devices. The results obtained from this analysis show excellent accuracy results, in the range of few nanoseconds and also standard deviation of less than 10 nanoseconds.**

I. Introduction

Time critical communications in Substation Automation Systems (SAS) based on Generic Object Oriented Substation Events (GOOSE) messages and Sample Values (SMV) as defined in IEC 61850 family of standards, need sub-microsecond synchronization for protection and control functions. The IEC Smart Grid Strategy Group recommends the Precision Time Protocol (PTP) as defined in IEEE 1588-2008 standard for high precision time synchronization in substations.

The precision of the synchronization in PTP systems depends on the precision of the timestamps. Compared to pure software solutions, the hardware assisted approaches timestamp messages at the phyter interface (GMII/MII) and reach higher accuracies. Therefore, using Intellectual Property (IP) Cores and Field Programmable Gate Arrays (FPGAs) seems to be the most precise and accurate method for implementing System-on-Chip (SoC) solutions capable of timestamping PTP messages in hardware. FPGAs offer hardware processing capabilities to achieve low switching latency times and flexibility enough to adapt the design to specific customer requirements, protocols updates and complex protocols combinations (eg. HSR and IEEE 1588). Besides IP business is mature for FPGAs allowing short time-to-market, nowadays, the technology offered by reconfigurable logic is moving forward to the next level: cost-affordable System-on-Chip devices such as the Zynq device by Xilinx, which has a double core Cortex-ARM9 with powerful peripheral on silicon (Gigabit Ethernet, memory controllers, CAN bus, etc.) and last-generation 28nm reconfigurable logic. This powerful platform enables to the industry and to the research community new possibilities in the field of Reliable Networks fully combined with IEEE 1588.

II. Experimental setups

The Test Setup A consists of two ZedBoard Zynq-7000 All Programmable SoC connected through an Ethernet link: the PTP master and the slave. In contrast, in the Test Setup B a Meinberg LANTIME M600/MRS/PTP reference time source was used as a professional PTP master. For each Test Setup two cases were analysed.

A. Case 1: Zynq PS GMAC IEEE1588-aware only

In this case, the Zynq device without any specific logic to support PTP on the Programmable Logic (PL) section, makes use of the IEEE 1588 support of the GMAC peripherals. Although better accuracy than using software timestamping is achieved, the timestamp register of this GMAC is not available directly for the logic implemented on the PL, limiting user-event timestamping by hardware or the generation of synchronized signals like PPS. In order to measure the precision of the protocol in such scenario, a PPS signal had to be generated via SW from a user space application.

B. Case 2: Zynq PS GMAC IEEE1588-aware combined with a IEEE1588 IP on PL

In this second case, additional logic is implemented on the PL section. This IP takes benefit from the IEEE1588 logic on the GMAC and adds support for synchronized signals generation by hardware (like PPS signal), as well as gives access to user-logic to the IEEE1588 synchronized timer, enabling hardware timestamping of user-events. The IP Core generates a high quality PPS output that can be routed to a PL GPIO. Hence, in this case, the PL section also had to be programmed.

III. Conclusions

While the digital offset shown by user application where close to zero nanoseconds, the PPS signals delay in Case 1 was higher than 1 microsecond with standard deviations in the range of hundred of microseconds. This delay is due to the jitter introduced by software when synchronizing system clock and changing the PS GPIO state of the PPS output. With the help of an IEEE 1588 IP Core in the PL section, as in the Case 2, PPS signals can be generated very precisely in hardware. Thus, offset measurement precision is hugely improved achieving accuracies in the range of 40 nanoseconds and standard deviations lower than 10 nanoseconds.

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