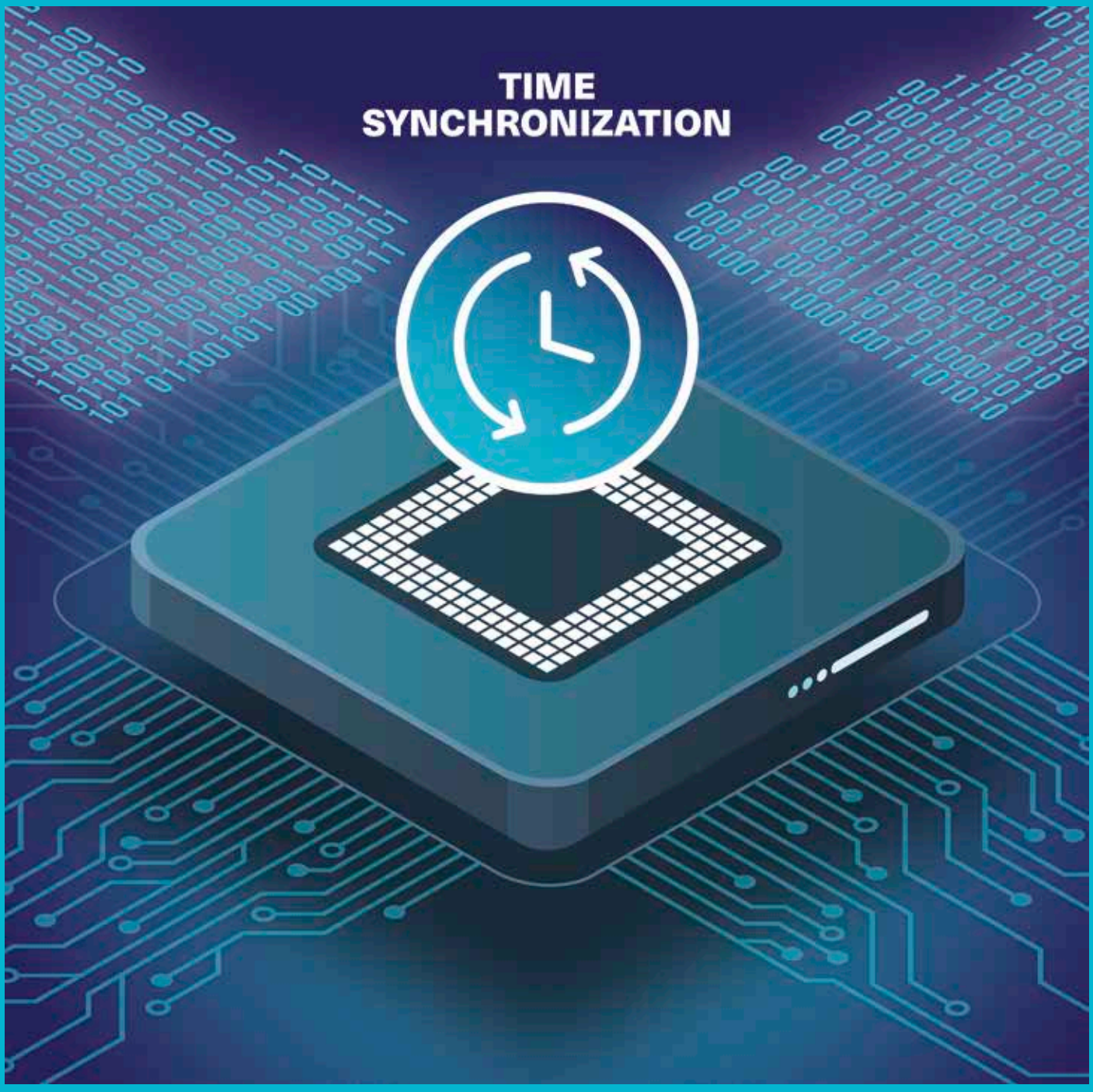
SocTek® IP Cores



1588Tiny IP Core

1588Tiny

Overview

1588Tiny is a hardware-only (VHDL) IP Core that implements an IEEE1588-2008 (Version 2) PTP slave / time receiver clock for FPGA. It provides submicrosecond clock synchronized to the network PTP Master.

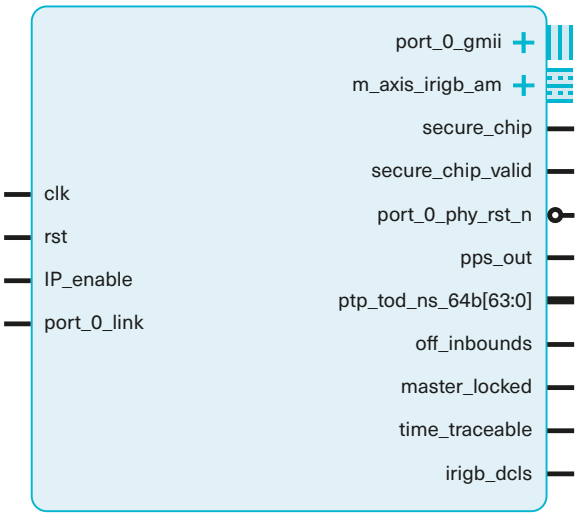
This solution does not require the use of an external PTP software stack running on an embedded CPU. It's an all-in-one PTP slave implementation.

It provides an excellent trade-off between a good enough clock accuracy and limited hardware resources (gates, memory, etc...) in a standalone product.

Key Features

- Multi-PTP profile capable: designed to support Default and Power Utility profile (IEC/IEEE 61850-9-3) with multiple configurations (layer-2/layer-3, E2E/P2P, etc...).
- PTP slave / time receiver to IRIG-B master / time transmitter bridge functionality: provides an IRIG-B (DCLS modulation) master reference using the internal PTP Timer as its time source.
- Dual port (passthrough) mode: avoids consuming the Ethernet port strictly for PTP communication by enabling a second Ethernet port.
- Event timestamping and alarm detection supported: based on the PTP timer clock, allowing the user to retrieve timestamps directly from a register.
- Fast & Smooth Integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite).
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™QSGMII IP core respectively
- 10/100/1000 Mbps AXI-S interface with a data width of 8 bits @ 125 MHz

Time Synchronization

- 64bit nanoseconds and 48bit seconds / 32bit nanoseconds selectable ToD PTP Clock output
- One pulse per second (PPS) output available
- Layer-2 (PTP over Ethernet) and Layer-3 (PTP over UDP) supported
- Event timestamping supported (up to 4 different events simultaneously)
- Alarm detection supported (up to 4 different alarms simultaneously)
- Optional IRIG-B master output synchronized with the PTP internal timer:
  - IRIG 200-04 compliant time synchronization master
  - Support for DCLS modulation
  - Support for all IRIG-B coded expressions, including year information, control functions and straight binary seconds
  - IEEE1344 extension support
  - Output type (IRIG-B time code) configurable both before implementation and on the fly
  - Generic DAC controller implementable compatible with SPI, QSPI and MICROWIRE protocols

Network Management & Monitoring

- IGMP version 2 protocol supported for layer-3 (PTP over UDP) operation, allowing 1588Tiny to join multicast IPv4 networks
- Per port MAC statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environ-ments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Evaluation & Design-in Kit

Description

The MEZU-A7G8 brick provides an out-of-the-box set-up that allows plug & play evaluation of 1588Tiny IP Core. The evaluation board can be provided with a preloaded bitstream that includes an instance of 1588Tiny IP Core configured for evaluation purposes. It is powered by an AMD/Xilinx Artix®-7 FPGA.

This hardware can also be used later as a development platform, what allows to shorten the development phase.

MEZU-A7G8 brick consists of the following package

- MEZU-A7G8 module (1x)
- Carrier board (1x)
- Reference bitstream preloaded into non-volatile storage (1x)
- Power supply (1x)
- Fibre / copper SFP modules (optional, purchased separately)

Related Products

- PreciseTimeBasic (PTB IP Core)

Ordering Code

Ordering code
S-3114 (1588Tiny IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

1588Tiny

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SOC-E®

www.soc-e.com
info@soc-e.com

Calle Islas Canarias 19, piso -1
48015 Bilbao (Spain)