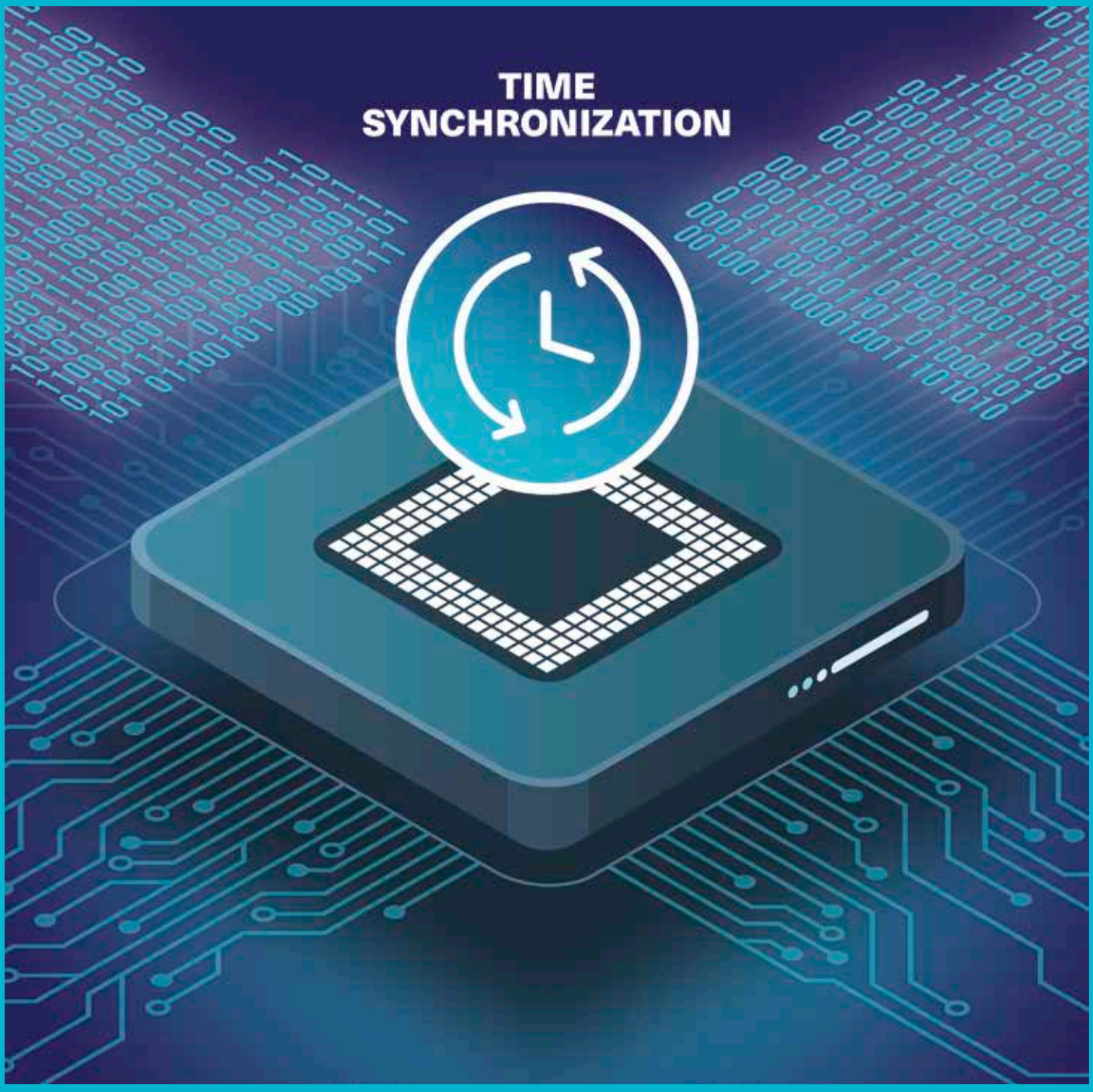
SocTek® IP Cores



IRIGtimeS IP Core

ITS

Overview

ITS is an IRIG 200-04 compliant time synchronization slave / time receiver for FPGA. This IRIG-B slave / time receiver IP has been designed to support multiple IRIG-B coded expressions as well as DCLS modulation in order to provide maximum flexibility.

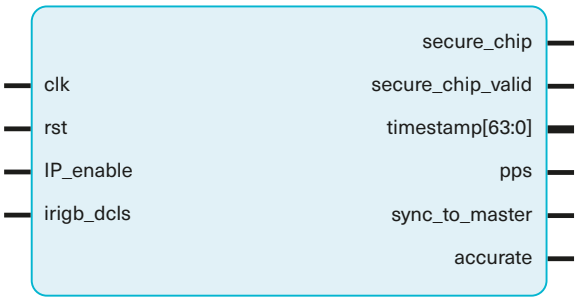
ITS can be configured to support the most extended IRIG-B time codes to provide higher compatibility with the majority of IRIG-B masters / time transmitters in the market. This configuration can be done before implementing the IP by selecting the desired modulation type, carrier frequency, coded expression and other parameters in the FPGA design tool as well as during runtime using register based configuration.

It has been designed as a hardware-only (VHDL) IP Core. No microprocessor or software is required in order to reduce integration complexity.

Key Features

- Multiple time code support: including year information, control functions and straight binary seconds.
- PPS and 10MHz inputs available: for synchronizing to high precision external clocks.
- IEEE1344 extension supported.
- Fast & smooth Integration: GUI available for FPGA vendor tools (i.e., AMD Vivado™ Design Suite).
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Time Synchronization

- IRIG 200-04 compliant time synchronization slave
- Support for DCLS modulation
- Input type (IRIG-B time code) configurable both before implementation and on the fly
- Sub-microsecond synchronization with the IRIG-B master
- 64-bit internal timer synchronized in time and frequency with the IRIG-B master
  - 32-bit for timestamp in seconds and 32-bit for nanoseconds

Management & Monitoring

- AXI4-Lite or UART management interfaces to access control registers (selectable at synthesis time)

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Related Products

- Master IRIG-B (IRIGtimeM IP Core)

Ordering Code

Ordering code
S-3119 (IRIGtimeS IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

ITS

IRIGtimeS IP Core

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