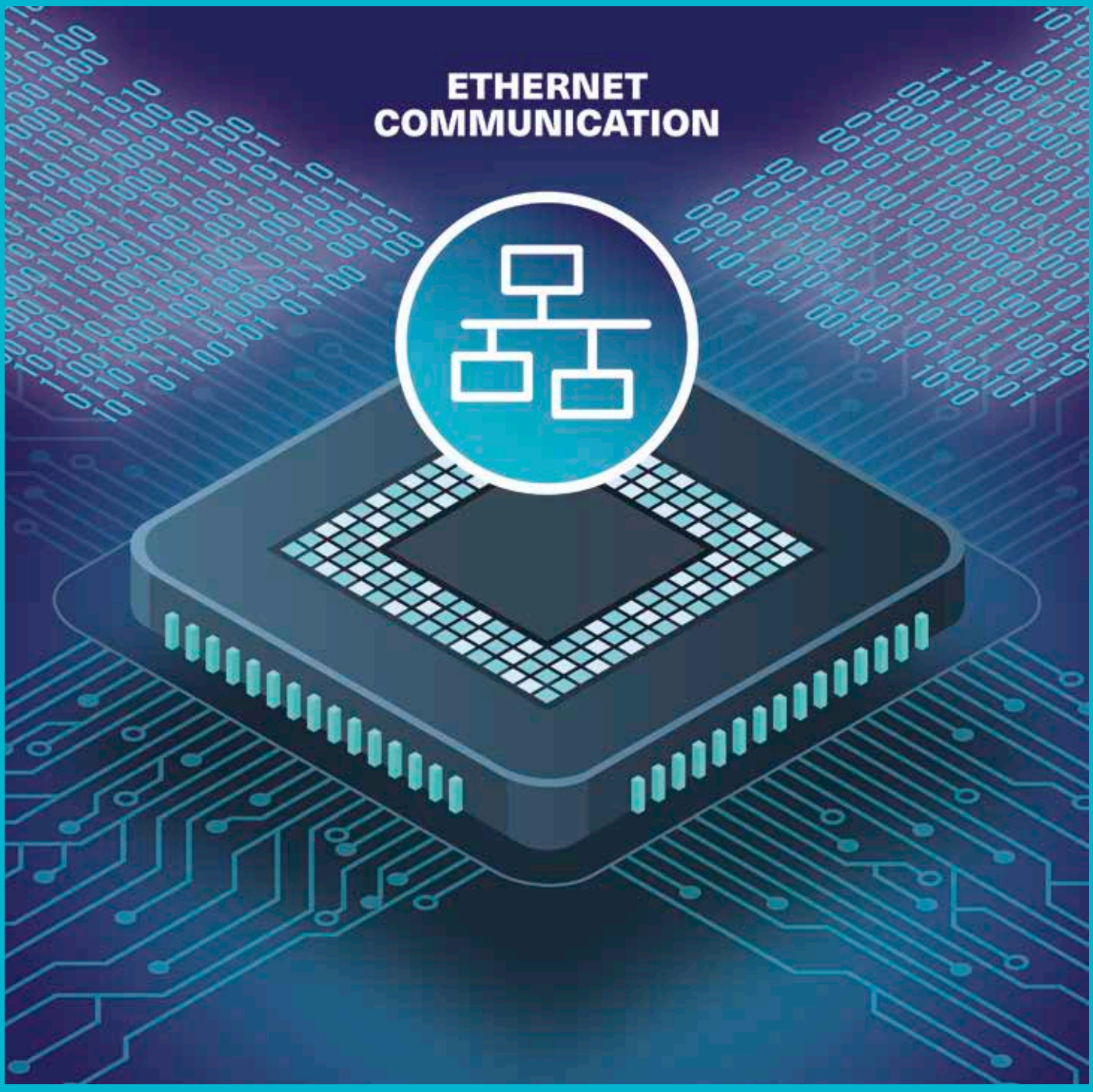
SocTek® IP Cores



10M/100M/1G Managed
Redundant Switch IP Core

MRS

Overview

MRS is an IP Core product that combines SOC-E MES IP Core and HPS IP Core in a single product. This implementation allows to combine regular ethernet ports with HSR/PRP capable ports in an easy way.

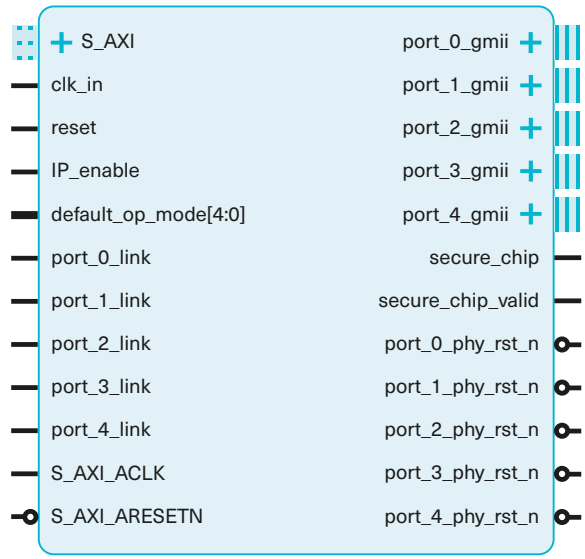
MRS implements a multi-port, multi-rate managed ethernet switch with a rich set of layer-2 configurable features as well as user selectable ports supporting High-availability Seamless Redundancy and Parallel Redundancy Protocol (HSR and PRP, IEC 62439-3 Clause 5 and 4 respectively) Edition 4.0 protocols for Reliable Ethernet communications providing zero recovery time.

All these characteristics enable a wide number of applications/sectors where the use of MRS IP Core is key. Automotive, Marine, Aerospace, Defence or Electric are examples of markets where our customers are already applying this technology.

Key Features

- Ethernet switch IP “builder”: hundreds of user-configurable parameters allow obtaining the exact switch configuration required by the customer, ensuring efficient use of the available programmable logic resources.
- Zero recovery time redundancy protocol support: the IP core implements HSR and PRP redundancy protocols (IEC 62439-3) providing seamless Ethernet redundancy.
- Different data-rate per port: each port speed and interface can be assigned independently.
- High-performance: up-to 1G interfaces without HOL (Head-of-line) blocking effect.
- Fast & smooth Integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite) Drivers & software components included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, RMII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™ QSGMII IP core respectively
- 10/100/1000 Mbps AXI-Stream interface with a data width of 8 bits @ 125 MHz
- Half-duplex support in 10/100Mbps PHY interface rates

Time Synchronization

- IEEE1588 (PTPv2): IEEE1588 Transparent Clock (TC) functionality (peer-to-peer) at layer-2 and layer-3 (IPv4)

Traffic Management

- Integrated ethernet switch fabric supporting up to 32 ports (number limited by the available resources on the device)
- Cut-through forwarding between HSR redundant ring ports for a very low forwarding latency independent from frame size
- HoLB (Head of Line Blocking) free switch fabric
- Shared dynamic and static filtering database. Implements hardware MAC address learning/ageing and look-up for up-to 9K absolute MAC addresses (synthesis scalable) at wire speed
- Independent VLAN Learning support for MAC address learning
- Searchable MAC addresses (and associated information) contained in the filtering database
- Programmable frame forwarding port mask to restrict frame forwarding towards port(s)
- Programmable EtherType based frame forwarding to restrict frame forwarding towards port(s)
- Static multicast frame filtering
- IGMP v1/v2 snooping1 (IPv4) support for multicast frame filtering
- Standard Frame size support (1518) or Jumbo frames up to 9 kByte (depends on memory availability)

Quality of Service

- Up to 8 priority queues per port (synthesis option)
  - Priority classification based on Ingress Port, PCP bits (802.1p), DSCP TOS bits of the IP packets (IPv4 TOS/IPv6 COS) and EtherType
  - Programmable remapping from PCP or DSCP fields to internal priority queues on a per-port basis
  - Programmable priority regeneration on a per-port basis
  - Egress traffic prioritization based on strict priority or Weighted Round Robin (WRR) scheduling algorithm
- IEEE 802.1Q tag-based and port-based VLANs. VLAN manipulation functions on reception (VLAN insertion) and transmission (VLAN removal/overwrite)
- MAC level ingress frame filtering based of destination MAC address and/or EtherType on per port basis
- Token bucket based ingress throughput rate limiting on per port basis
- MAC level ingress frame rate limiting on per port basis
- Credit Based Shaper egress throughput rate limiting on per port basis
- Egress frame rate limiting on per port basis
- Broadcast/Multicast storm protection

Network Management & Monitoring

- IEEE 802.1D Spanning-Tree Protocol (STP) to prevent loops from being formed when switches or bridges are interconnected via multiple paths
- IEEE 802.1w Rapid Spanning Tree Protocol (RSTP) provides rapid convergence of spanning tree
- IEEE 802.1s Multiple Spanning Tree Protocol (MSTP) provides link availability in multiple VLAN environments by allowing multiple spanning trees
- Multisession port mirroring capabilities. Ingress and egress mirroring functions to allow copying of frames to a mirror port. Option for mirroring only filtered frames that match a specific data pattern.
- User/network port-level security via IEEE802.1X authentication and MAC-based filtering
- Host access control for only frames specified by the user (destination MAC and/or EtherType based)
- Per port MAC and switch statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)
- I2C master interface for external device configuration (i.e. an EEPROM memory with non-volatile configuration)

Ring Redundancy Protocols

- High-availability Seamless Redundancy (HSR). It can operate in any of the following modes, which are changeable at runtime:
  - Mode H (mandatory, default mode): HSR-tagged forwarding
  - Mode M (optional): mixed forwarding HSR-tagged and non HSR-tagged
  - Mode N (optional): no forwarding
  - Mode T (optional): transparent forwarding
  - Mode U (optional): unicast forwarding
  - Mode R (optional): for RedBoxes to be connected to an RSTP bridge
- Parallel Redundancy Protocol (PRP). It can operate in any of the following modes, which are changeable at runtime:
  - Duplicate Discard (default mode)
  - Duplicate Accept (testing only)
- Media Redundancy Protocol (MRP) for ring topology networks: Media Redundancy Manager (MRM) and Media Redundancy Client (MRC) modes
- Device Level Ring (DLR) redundancy protocol for EtherNet/IP: ring Supervisor node to control DLR network and Beacon based node to process Beacon frames

Others

- Distributed Switch Architecture (DSA) frame tagging to merge application specific messages to management port and to distribute application specific messages to a specific port
- Exclusive forwarding of known protocol specific frames or custom frames to/from management port

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity/Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted/Source RTL code
- Software components: drivers, configuration API & SW stacks
- Documentation (IP Core and software components)
- (Optional) Networking Testbench Suite (NTS)
- (Optional) AMD Vivado™ design suite example design

Evaluation & Design-in Kit

Description

The SMARTmpsoc and SMARTzynq Brick provide an out-of-the-box set-up that allows plug & play evaluation of MRS IP Core. The evaluation board is provided with a preloaded firmware that includes an instance of SOC-E IP Core(s) plus additional software components that are executed in the processing system (CPU) of the platform. Linux OS is loaded in the evaluation firmware.

This hardware can also be used later as a development platform, what allows to shorten the development phase.

SMARTmpsoc Brick consists of the following package

- SMARTmpsoc module (1x)
- Carrier board (1x)
- Reference firmware (predefined image) preloaded into non-volatile eMMC storage (1x)
- Power supply (1x)
- Fibre/Copper SFP modules (optional, purchased separately)

SMARTzynq Brick consists of the following package

- SMARTzynq module (1x)
- Carrier board (1x)
- Reference firmware (predefined image) preloaded into non-volatile microSD card storage (1x)
- Power supply (1x).
- Fibre/Copper SFP modules (optional, purchased separately)

Related Products

- Networking Testbench Suite (NTS)
- 1G HSR/PRP Switch (HPS IP Core)
- 1G Managed Ethernet Switch (MES IP Core)

Ordering Code

Ordering code
S-3124 (MES IP Core)
EVB07.27 (SMARTmpsoc Brick)
EVB04.28 (SMARTzynq Brick)

To know more about other available references, please contact your sales representative.

SocTek®

By

MRS

10M/100M/1G Managed
Redundant Switch IP Core

SOC-E®

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