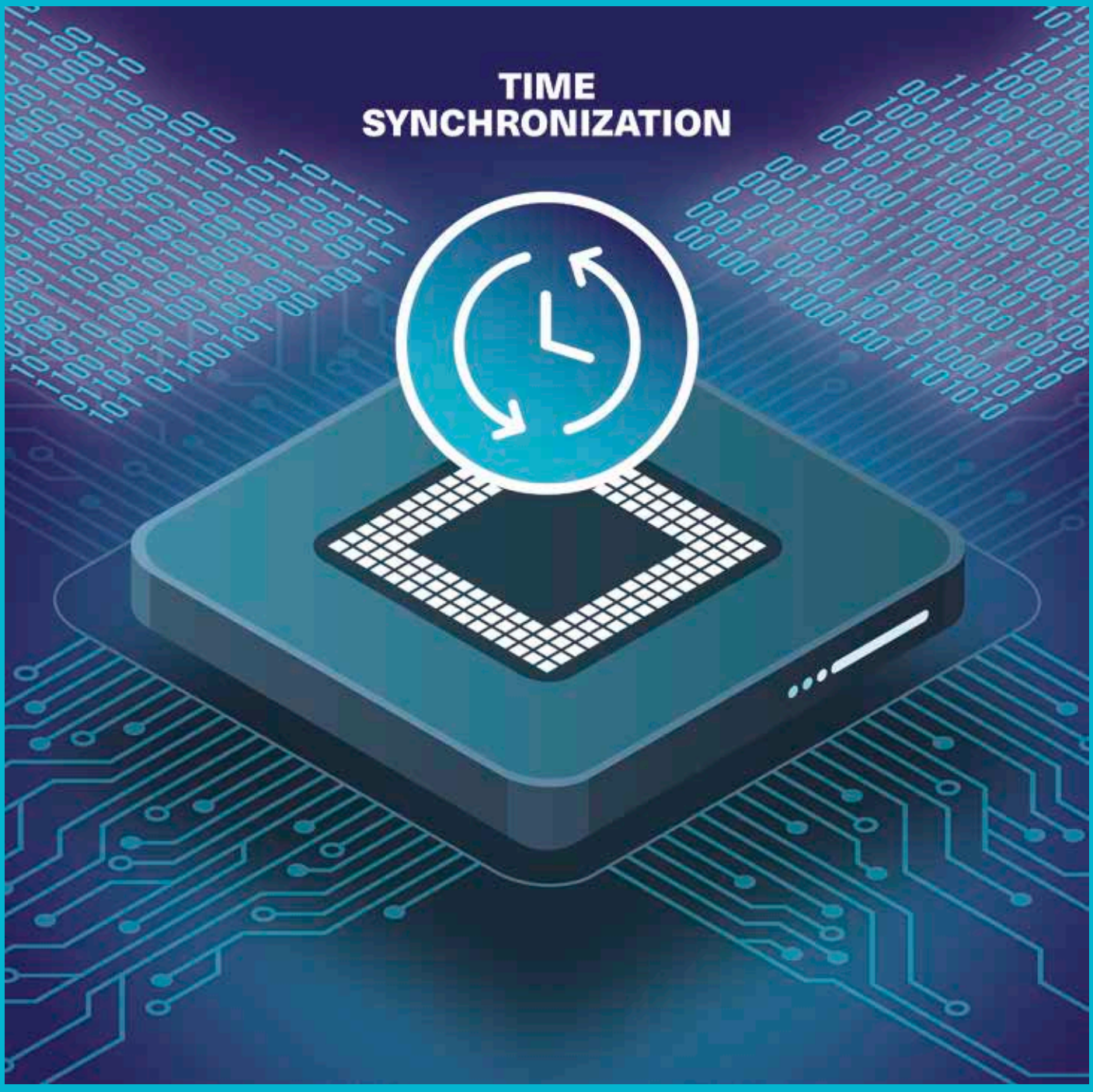
SocTek® IP Cores



PreciseTimeBasic IP Core

PTB

Overview

PreciseTimeBasic is a PTP Ordinary (master / time transmitter & slave / time receiver) capable clock for System-on-Programable Chip (SoPC). As a time receiver it provides nanosecond level clock synchronized to network PTP time transmitter. As a time transmitter it generates all the required PTP frames.

This solution is composed by three main components: An IP Core for FPGA that implements the timestamping unit (TSU); a PTP stack for Linux operating system (running on the in-built SoPC processor) and a driver (provided as a patch for Linux kernel).

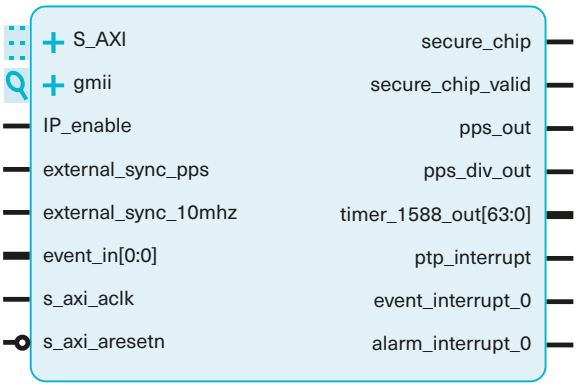
PreciseTimeBasic IP Core is specifically designed for AMD/Xilinx SoPC platforms, specifically Zynq®-7000 & Zynq®UltraScale+ MPSoC families.

This product provides higher accuracy and flexibility compared to SOC-E 1588Tiny IP Core by making use of a software PTP stack.

Key Features

- Multi-PTP profile capable: designed to support Default and Power Utility Profile (IEC/IEEE 61850-9-3) with multiple configurations (layer-2/layer-3, E2E/P2P, etc...).
- PTP time transmitter (master) and time receiver (slave) capable: both operation modes supported in the same implementation.
- Event timestamping and alarm detection supported: based on the PTP timer clock, allowing the user to retrieve timestamps directly from a register.
- Fast & smooth integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite). Drivers & software components included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™QSGMII IP core respectively
- Configurable AXI-Stream interfaces to support several data rates
  - 1000/10000/25000 Mbps AXI-S interface with a data width of 64 bits @ 156.25 MHz

Time Synchronization

- 32bit nanoseconds and 32bit seconds ToD PTP clock output
- One Pulse Per Second (PPS) output available
- One frequency selectable pulse output available (1kHz/ 2kHz/ 4kHz/ 8kHz/ 16kHz/32kHz)
- Layer-2 (PTP over Ethernet) and Layer-3 (PTP over UDP) supported
- Event timestamping supported (up to 4 different events simultaneously)
- Alarm detection supported (up to 4 different alarms simultaneously)

Network Management & Monitoring

- Per port MAC statistics for managing and debugging purposes
- AXI4-Lite management interfaces to access control and statistics registers

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity / Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted / Source RTL code
- Software components: drivers, configuration API & SW stacks
- Documentation (IP Core datasheet)
- (Optional) AMD Vivado™ design suite example design

Evaluation & Design-in Kit

Description

The SMARTmpsoc and SMARTzynq brick provide an out-of-the-box set-up that allows plug & play evaluation of PTB IP Core. The evaluation board is provided with a preloaded firmware that includes an instance of SOC-E IP Core(s) plus additional software components that are executed in the processing system (CPU) of the platform. Linux OS is loaded in the evaluation firmware.

This hardware can also be used later as a development platform, what allows to shorten the development phase.

SMARTmpsoc brick consists of the following package

- SMARTmpsoc module (1x)
- Carrier board (1x)
- Reference firmware (predefined image) preloaded into non-volatile eMMC storage (1x)
- Power supply (1x)
- Fibre / copper SFP modules (optional, purchased separately)

SMARTzynq brick consists of the following package

- SMARTzynq module (1x)
- Carrier board (1x)
- Reference firmware (predefined image) preloaded into non-volatile microSD card storage (1x)
- Power supply (1x)
- Fibre / copper SFP modules (optional, purchased separately)

Related Products

- 1588Tiny IP Core

Ordering Code

Ordering code
S-3101 (PTB IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

PTB

PreciseTimeBasic IP Core

SOC-E®

www.soc-e.com
info@soc-e.com

Calle Islas Canarias 19, piso -1
48015 Bilbao (Spain)