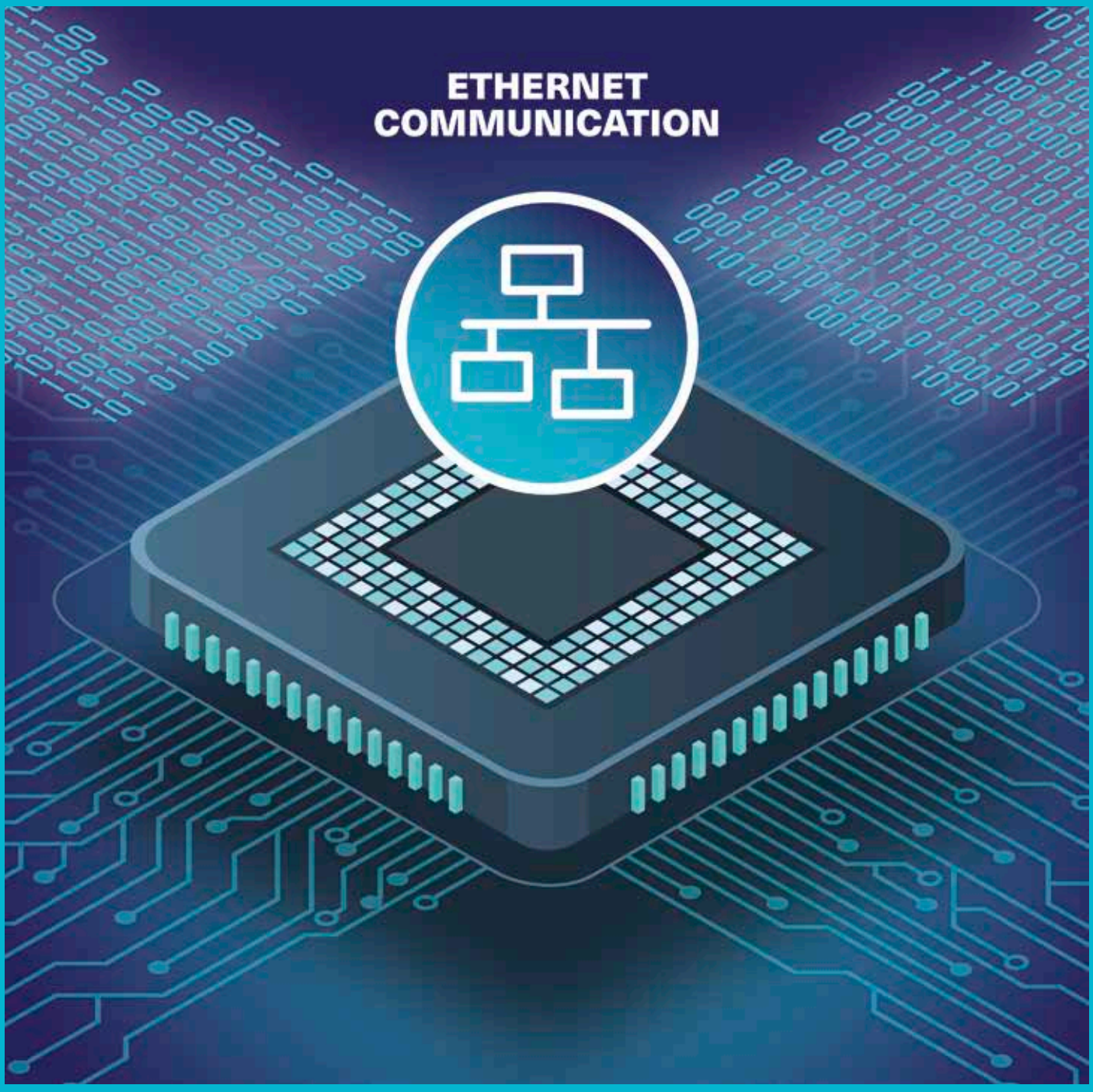
SocTek® IP Cores



10M/100M/1G/10G Managed/Unmanaged
(TSN) Ethernet Switch IP Core

TGES

Overview

TGES is a multi-port, multi-rate managed Ethernet switch with Time-Sensitive Networking (TSN) capabilities.

TGES has a rich set of configurable parameters, both at synthesis time & during runtime, in order to optimize the logic resources footprint attending to the specific user needs. These generics can be configured graphically through the Vivado GUI as well.

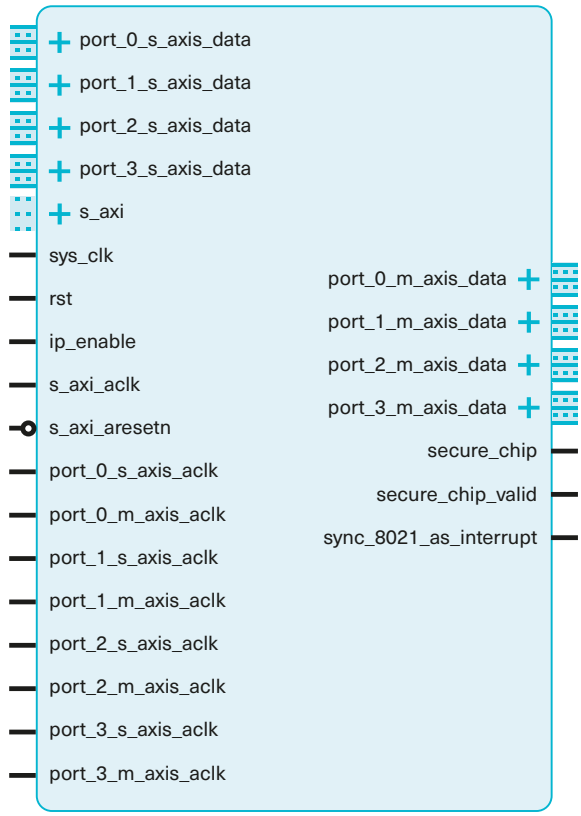
The internal micro-architecture includes disruptive enhancements in order to ensure a reliable operation of the switch even in critical use-cases.

All these characteristics enable a wide number of applications/sectors where the use of TGES IP Core is key. Automotive, Marine, Aerospace, Defence or Electric are examples of markets where our customers are already applying this technology.

Key Features

- Time-Sensitive Networking (TSN) support: aligned with the different TSN profiles, such as Aerospace (P802.1DP), Automotive (P802.1DG) or Industrial Automation (IEC/IEEE 60802).
- Ethernet switch IP “builder”: hundreds of user-configurable parameters allow obtaining the exact switch configuration required by the customer, ensuring efficient use of the available programmable logic resources.
- Different data-rate per port: each port speed and interface can be assigned independently.
- High-performance: up-to 10G interfaces without HOL (Head-of-line) blocking effect.
- Fast & smooth integration: GUI available for some FPGA vendor tools (i.e., AMD Vivado™ Design Suite). Drivers & software components included as part of the product deliverable.
- Evaluation version available: encrypted, time-limited version available.

GUI Block Diagram



Technical Specifications

Communication Interfaces

- Integrated 10M/100M/1000M MACs for 10/100 Mbps and 1 Gbps PHY interface rates to use with any PHY interface type (e.g. MII, GMII, RGMII) depending on application
- Compatible with SGMII (Serial Gigabit Media Independent Interface) or QSGMII (Quad Serial Gigabit Media Independent Interface) PHY interfaces throughout an internal GMII based connection to AMD LogiCORE™ SGMII IP core and LogiCORE™ QSGMII IP core respectively
- Configurable AXI-Stream interfaces to support several data rates:
  - 10/100/1000 Mbps AXI-S interface with a data width of 8 bits @ 125 MHz
  - 10/100/1000/2500/5000/10000 Mbps AXI-S interface with a data width of 32 bits @ 312.5 MHz
  - 10/100/1000/2500/5000/10000 Mbps AXI-S interface with a data width of 64 bits @ 156.25 MHz
- Compatible with USXGMII (Universal Serial 10GE Media Independent Interface) or 10GBASE-R PHY interfaces throughout an internal AXI-S based connection to AMD LogiCORE™ USXGMII IP core and LogiCORE™ 10G/25G Ethernet Subsystem IP core respectively

Time-Sensitive Networking (TSN)

- TSN features can be enabled/ disabled independently
- IEEE 802.1AS - Timing and Synchronization
- IEEE 802.1Qav - Credit Based Shaper (CBS)
- IEEE 802.1Qbv - Time Aware Shaper (TAS)
- IEEE 802.1Qci - Per-Stream Filtering and Policing
- IEEE 802.1CB - Frame Replication and Elimination for Reliability (FRER)
- IEEE 802.1Qcc - Stream Reservation Protocol (SRP) Enhancements and Performance Improvements

Time Synchronization

- Time synchronization according to IEEE 802.1AS-2020 and IEEE1588 (PTP)
  - Up to four IEEE802.1AS time domains
- Legacy PTP: IEEE1588 Transparent Clock (TC) functionality (End-to-End or Peer-to-peer) at layer-2 and layer-3 (IPv4 and IPv6)
- Legacy PTP: IEEE 1588 Boundary Clock (BC) at layer-2 and layer-3 (IPv4 and IPv6)

Traffic Management

- Integrated Ethernet switch fabric supporting up to 32 ports (number limited by the available resources on the device)
- HoLB (Head of Line Blocking) free switch fabric
- VOQ (Virtual Output Queue) based frame storage to prevent HoLB effect
- Resource sharing algorithm (executed at synthesis time) to define the optimal internal architecture to reduce resource usage without performance compromises
- Shared dynamic and static filtering database. Implements hardware MAC address learning/ageing and look-up for up to 9K absolute MAC addresses (synthesis scalable) at wire speed
- Independent VLAN learning support for MAC address learning
- Searchable MAC addresses (and associated information) contained in the filtering database
- Programmable frame forwarding port mask to restrict frame forwarding towards port(s)
- Static multicast frame filtering
- IGMP v1/v2 snooping1 (IPv4) support for multicast frame filtering
- Standard frame size support (1518) or Jumbo frames up to 9 kByte (depends on memory availability)

Quality of Service

- Up to 8 priority queues per port (synthesis option)
  - Priority classification based on PCP bits (802.1p)
  - Egress traffic prioritization based on strict priority scheduling algorithm
- IEEE 802.1Q tag-based and Port-based VLANs. VLAN manipulation functions on reception (VLAN insertion) and transmission (VLAN removal/overwrite)
- Token bucket based ingress and egress traffic rate limiting on per port basis
- Broadcast/Multicast storm protection

Network Management & Monitoring

- IEEE 802.1D Spanning-Tree Protocol (STP) to prevent loops from being formed when switches or bridges are interconnected via multiple paths
- IEEE 802.1w Rapid Spanning Tree Protocol (RSTP) provides rapid converge of spanning tree
- IEEE 802.1s Multiple Spanning Tree Protocol (MSTP) provides link availability in multiple VLAN environments by allowing multiple spanning trees
- Port mirroring capabilities. Ingress and egress mirroring functions to allow copying of frames to a mirror port. Option for mirroring only filtered frames that match a specific data pattern
- Per port MAC and switch statistics for managing and debugging purposes
- Wide range of management interfaces to access control and statistics registers (selectable at synthesis time)
- I2C master interface for external device configuration (i.e. an EEPROM memory with non-volatile configuration)

Others

- Distributed Switch Architecture (DSA) frame tagging to merge application specific messages to management port and to distribute application specific messages to a specific port
- Exclusive forwarding of known protocol specific frames or custom frames to/from management port

Technical Support, Verification & Deliverables

Technical Support

IP Licenses are provided along with a technical support package that ensures a direct communication channel with our highly experienced support engineers. This is vastly valued during customer product development & integration phases.

Verification

All our IP Cores are rigorously tested, hardware-validated and verified in real-life environments. A 3-phase based IP product verification is applied:

- Entity/Block-oriented simulation
- Global-oriented simulation
- In-hardware validation

Deliverables

- Encrypted/Source RTL code
- Software components: drivers, configuration API & SW stacks
- Documentation (IP Core and software components)
- (Optional) Networking Testbench Suite (NTS)
- (Optional) AMD Vivado™ design suite example design

Related Products

- Networking Testbench Suite (NTS)
- TSN EndPoint (ETSN IP Core)
- 1G TSN Ethernet Switch (MTSN IP Core)
- 1G Managed Ethernet Switch (MES IP Core)

Ordering Code

Ordering code
S-3135 (TGES IP Core)

To know more about other available references, please contact your sales representative.

SocTek®

By

TGES

10M/100M/1G/10G Managed/Unmanaged
(TSN) Ethernet Switch IP Core

SOC-E®

www.soc-e.com
info@soc-e.com

Calle Islas Canarias 19, piso -1
48015 Bilbao (Spain)